

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-187342

(43)Date of publication of application : 09.07.1999

(51)Int.Cl.

H04N 5/78

G11B 20/10

H04N 5/92

(21)Application number : 09-351569

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(22)Date of filing : 19.12.1997

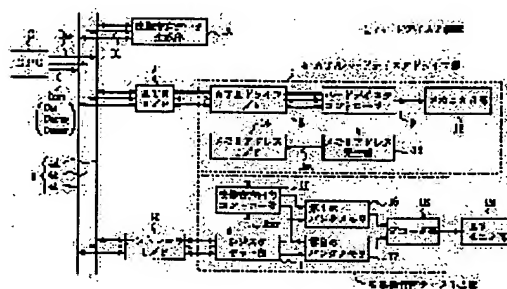
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(54) DATA PROCESSING METHOD AND DATA PROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To improve a transfer rate by designating a first address in a first storage means to store transmitted video data for every frame, designating the second address based on the first address to store video data for every frame and reading video data from the second storage means for every frame by means of the synchronization with a writing timing to display it.

SOLUTION: CPU 2 designates the address corresponding to address data DAD and, after that, generates the addresses corresponding to a first bank memory and the second bank memory 17 in a video voice data output part 6 based on the address. The generated addresses are alternately designated, audiovideo data D1 is written in one of the first bank memory 16 of the second one 17 by frame unit, audiovideo data D1 is read from the other one by frame unit and it is displayed on the screen of an AV monitor part 19. Thus, screen display is enabled by synchronizing with the timing by which audiovideo data D1 is written on a hard disk.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

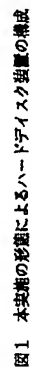
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(11)特許出願公開番号



【特許請求の範囲】

【請求項1】外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1のステップと、

上記第1の記憶手段に指定された上記第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成する第2のステップと、

上記第2の記憶手段に上記第2のアドレスを指定して上記映像データを上記フレーム毎に記憶する第3のステップと、

上記記録媒体に書き込むタイミングに同期して、上記第2の記憶手段から上記映像データを上記フレーム毎に読み出して画面表示する第4のステップとを具えることを特徴とするデータ処理方法。

【請求項2】上記第2のステップでは、上記第2の記憶手段は第1及び第2のバンクメモリを有し、

上記第3及び第4のステップでは、上記第2のアドレスを上記第1又は第2のバンクメモリに交互に指定して、上記第1又は第2のバンクメモリのうち一方に上記映像データを上記フレーム毎に記憶すると共に、他方から上記映像データを上記フレーム毎に読み出して画面表示することを特徴とする請求項1に記載のデータ処理方法。

【請求項3】外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1の記憶制御手段と、

上記第1の記憶制御手段によつて指定された上記第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成するアドレス生成手段と、

上記第2の記憶手段に上記アドレス生成手段によつて生成された上記第2のアドレスを指定して上記映像データを上記フレーム毎に記憶する第2の記憶制御手段と、

上記第1の記憶手段から上記映像データを上記フレーム毎に読み出して記録媒体に書き込む書込手段と、

上記書込手段が上記記録媒体に書き込むタイミングに同期して、上記第2の記憶手段から上記映像データを上記フレーム毎に読み出して画面表示する表示手段とを具えることを特徴とするデータ処理装置。

【請求項4】上記第2の記憶手段は、第1及び第2のバンクメモリを有し、

上記第2の記憶制御手段は、上記アドレス生成手段によつて生成された上記第2のアドレスを上記第1又は第2のバンクメモリに交互に指定して、上記第1又は第2のバンクメモリのうち一方に上記映像データを上記フレーム毎に書き込むと共に、他方から上記映像データを上記フレーム毎に読み出して上記表示手段に表示することを特徴とする請求項3に記載のデータ処理装置。

【発明の詳細な説明】

【0001】

【目次】以下の順序で本発明を説明する。

【0002】発明の属する技術分野

従来の技術

発明が解決しようとする課題

課題を解決するための手段

発明の実施の形態

(1) ハードディスク装置の全体構成(図1～図4)

(2) データ書込み処理手順(図5)

(3) 本実施の形態の動作及び効果

(4) 他の実施の形態(図6～図7)

発明の効果

10 【0003】

【発明の属する技術分野】本発明はデータ処理方法及びデータ処理装置に関し、例えば映像音声データの書込み及び読出しを行うハードディスク装置に適用して好適なものである。

【0004】

【従来の技術】従来、この種のハードディスク装置として、複数のハードディスクを同軸中心上に高速回転させながら、複数の可動アームの先端に取り付けられた磁気ヘッドをそれぞれハードディスクの一面又は他面に対応させて、当該各ハードディスクの両面上にそれぞれ映像音声データを必要に応じてデータ圧縮して記録するようにしたものを用いられている。

【0005】これら各ハードディスクの両面にはそれぞれ同心円状にトラックが形成され、最外周から最内周に向かつてトラック番号が割り当てられている。さらに各トラックは、所定のデータ長を単位とするセクタに分割され、当該各セクタにはセクタ番号としての論理ブロックアドレス(LBA)が割り当てられている。

30 【0006】このハードディスク装置において、CPUは、所定のハードディスクの各セクタ毎に割り当てられた論理ブロックアドレスに応じてディスクドライブ内に設けられたデータレジスタを指定すると共に、当該各セクタのセクタ転送回数を表すセクタカウント数をデータレジスタに設定する。

【0007】続いてCPUは、複数のセクタからなる一連の映像音声データを1映像音声データブロック毎の、例えば1フレーム毎に順次バンク切替方式の各バッファメモリに交互にFIFO(First In First Out)の順で各データブロックを書き込んだ後、ディスクドライブ内のデータレジスタに対して順次アドレス指定しながら映像音声データを1フレーム毎に書き込むようになされている。

【0008】この後、CPUは、バッファメモリから読み出した映像音声データを、映像音声出力回路に内蔵されたメモリに対して順次アドレス指定しながら1フレーム毎に書き込んだ後、必要に応じて当該メモリから読み出して外部接続されたモニタ装置に出力するようになされている。

【0009】

50 【発明が解決しようとする課題】ところで、バッファメ

メモリに格納された一連の映像音声データをディスクドライブ及び映像音声出力回路の両方に同時にデータ転送する場合、CPUは、ディスクドライブ内のデータレジスタ及び映像音声出力回路内のメモリに対して同一のアドレスを直接指定することができず、互いに異なるアドレスを順次指定しながらそれぞれ映像音声データをフレーム単位で転送しなければならなかった。

【0010】またCPUは、ディスクドライブに対してデータ転送を開始する前に当該ディスクドライブ内のデータレジスタ以外の種々のレジスタを設定する場合、当該レジスタの設定値が確定するまでの処理時間が毎回約100～300〔ns〕ずつかかっていた。さらにCPUは、ディスクドライブに対してデータ転送を終了した後にデータ割り込みの処理を複数回行くと、その度に約5～10〔μs〕前後の処理時間がかかっていた。

【0011】このため一連の映像音声データを連続してデータ転送する場合には、上述したレジスタ設定及び割り込み処理が行われることを考慮して、当該映像音声データを各フレーム単位毎に所定の時間以内（例えば128〔kbyte〕を33〔ms〕以内、また別の例では512〔kbyte〕を0.5〔ms〕以内）に転送させるようになされていた。

【0012】従つてCPUは、ディスクドライブに対して一旦データ転送を開始させると、途中で停止することなく各フレーム単位毎に映像音声データをデータレジスタに転送しなければならず、この後に映像音声出力回路に対して各フレーム単位の映像音声データをメモリに転送しなければならなかった。この結果、ディスクドライブ及び映像音声データ出力回路に対するデータ転送時間がそれぞれ長くなるという問題があった。

【0013】さらにCPUは、ディスクドライブに対してデータ転送する際に、ディスクドライブ内でリトライ（再書き込み）動作、ハードディスク上のトラック間ジャンプ又はセクタ間ジャンプ等の切換え動作等が行われた場合、当該各動作時にはディスクドライブからデータ転送を行う際の入出力可能状態信号D_{IO_{req}}を利用してその信号を一時的に停止するなどの、ATA標準方式に記載されている、CPUからのアクセス処理を一時的に待たせるためのアクセス待ち要求信号が発せられる。以上のこれらの結果、CPUは、ディスクドライブに対して時間的に不連続なデータ転送を行うこととなり、このためリアルタイム処理を行うためにはハードディスクでは通常のデータ転送レートよりも高速なデータ転送レートで行い、他方、映像音声出力回路では別処理により連続したデータ転送を行わなければならなかった。

【0014】このことはディスクドライブに対するデータ転送をリアルタイムではなく別時間で処理していることとなり、CPUはディスクドライブに対するデータ転送を確実に行うことができたか否かをリアルタイムで判断し難いという問題があった。

【0015】本発明は以上の点を考慮してなされたもので、転送レートを格段と向上し得るデータ処理方法及びデータ処理装置を提案しようとするものである。

【0016】

【課題を解決するための手段】かかる課題を解決するため本発明においては、外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1のステップと、第1の記憶手段に指定された第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成する第2のステップと、第2の記憶手段に第2のアドレスを指定して映像データをフレーム毎に記憶する第3のステップと、記録媒体に書き込むタイミングに同期して、第2の記憶手段から映像データをフレーム毎に読み出して画面表示する第4のステップとを設けるようにした。

【0017】この結果、映像データをフレーム毎に記録媒体に書き込むタイミングに同期して、当該書き込んだ映像データをフレーム毎にリアルタイムで画面表示することができる。

【0018】また本発明においては、外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1の記憶制御手段と、第1の記憶制御手段によつて指定された第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成するアドレス生成手段と、第2の記憶手段にアドレス生成手段によつて生成された第2のアドレスを指定して映像データをフレーム毎に記憶する第2の記憶制御手段と、第1の記憶手段から映像データをフレーム毎に読み出して記録媒体に書き込む書込手段と、書込手段が記録媒体に書き込むタイミングに同期して、第2の記憶手段から映像データをフレーム毎に読み出して画面表示する表示手段とを設けるようにした。

【0019】この結果、映像データをフレーム毎に記録媒体に書き込むタイミングに同期して、当該書き込んだ映像データをフレーム毎にリアルタイムで画面表示することができる。

【0020】

【発明の実施の形態】以下図面について、本発明の一実施の形態を詳述する。

【0021】（1）ハードディスク装置の全体構成
図1において1は全体としてIDE（intelligent drive electronics）インタフェイスの標準規格ATA（ATA attachment）方式からなるハードディスク装置を示し、CPU2によつて映像音声データ生成部3から順次供給される映像音声データD1をホストバス4を介してATAハードディスクドライブ部5及び映像音声データ出力部6にそれぞれデータ転送するようになされている。

【0022】ホストバス4及びATAハードディスクドライブ部5間にはATAインタフェイス部7が設けら

れ、CPU2及び映像音声データ生成部3から供給される種々のデータをATAハードディスクドライブ部5内のATAドライブインタフェイス部8を介してハードディスクコントローラ9に与えるようになされている。

【0023】またホストバス4及び映像音声データ出力部6間にはコントローラインタフェイス部10が設けられ、CPU2及び映像音声データ生成部3から供給される種々のデータを映像音声データ出力部6内のレジスタセット部11に与えるようになされている。

【0024】このホストバス4は、アドレスバス4A、データバス4B及びコントロールバス4Cからなる。このうちアドレスバス4Aは、CPU2から送出される種々のレジスタのアドレスを指定するためのアドレスデータ D_{A0} をATAインタフェイス部7及びコントローラインタフェイス部10に与えるためのバスである。

【0025】またデータバス4Bは、映像音声データ生成部3から供給される映像音声データD1をATAインタフェイス部7及びコントローラインタフェイス部10に与えるためのバスである。

【0026】さらにコントロールバス4Cは、CPU2から送出されるATAハードディスクドライブ部5内の各レジスタに対するデータ転送を制御するためのコントロールデータ D_{CON} をATAインタフェイス部7に与えると共に、当該データ転送のタイミングが不連続となる場合にATAハードディスクドライブ部5がデータ転送を一時的に停止するためにウェイト信号 D_{WA} をCPU2に対して送出するためのバスである。なおこのコントロールバス4Cは、ATAハードディスクドライブ部5内の各レジスタに対するデータ転送が終了したときに当該ATAハードディスクドライブ部5から割込み処理要求信号 D_{INTRQ} をCPU2に送出すると共に、当該データ転送の際にアクセス可能な状態であるときATAインタフェイス部7及びコントローラインタフェイス部10から入出力可能状態信号 D_{IORDY} をCPU2に送出するためのバスでもある。

【0027】ここでATAハードディスクドライブ部5内のハードディスクコントローラ9は、コマンドブロックレジスタRA及びコントロールブロックレジスタRBを有し、当該各レジスタRA、RBをCPU2から供給されたアドレスデータ D_{A0} に基づいてメカニカル部12内の所定のハードディスク（図示せず）の各セクタ毎に割り当てられたアドレスに応じて指定する。

【0028】このときATAインタフェイス部7は、CPU2からアドレスバス4Aを介して供給されるアドレスデータ D_{A0} に所定のアドレス変換処理を施すことにより、ハードディスクコントローラ9内のコマンドブロックレジスタRA及びコントロールブロックレジスタRBに対してアドレスデータ D_{A0} に応じたアドレスを指定し得るようになされている。

【0029】具体的にはアドレスデータ D_{A0} は、図2

(A)に示すように、それぞれ16進法表記の32ビットで表された複数のアドレス $A_0 \sim A_{10}$ から構成される。これら複数のアドレス $A_1 \sim A_{10}$ は、ATAインタフェイス部7を介してコマンドブロックレジスタRA及びコントロールブロックレジスタRBに対応するアドレスに変換される。

【0030】図2(B)に変換後のアドレスを示し、1ビットの「CS0-」及び「CS1-」と3ビットの「DA(デバイスアドレス)」とによつて表され、このうち「CS0-」及び「CS1-」は共に複数のレジスタの中から設定対象となるレジスタを選択するためのアドレスである。実際にアドレスデータ D_{A0} に基づく複数のアドレス $A_1 \sim A_{10}$ のうち、アドレス $A_1 \sim A_0$ は「CS0-」が値「0」でかつ「CS1-」が値「1」を表し、このときコマンドブロックレジスタRAが選択される。またアドレス A_9 及び A_{10} は「CS0-」が値「1」でかつ「CS1-」が値「0」を表し、このときコントロールブロックレジスタRBが選択される。

【0031】また「DA」は16進法表記の3ビットで表された「0h」から「7h」までの8種類のデバイスアドレスを示し、これらのデバイスアドレスに対応してコマンドブロックレジスタRA又はコントロールブロックレジスタRBを構成する各レジスタの種類が選択される。

【0032】このコマンドブロックレジスタRAには、データレジスタ R_1 、エラー/フイーチャレジスタ R_2 、セクタカウントレジスタ R_3 、論理ブロックアドレスレジスタ R_4 及びステータス/コマンドレジスタ R_5 があり、コントロールブロックレジスタRBには、アルタネートステータス/デバイスコントロールレジスタ R_6 及び不使用レジスタ R_7 がある。データレジスタ R_1 がワード単位で書込み又は読出し可能であるのに対して他のレジスタ $R_2 \sim R_7$ はバイトレジスタ単位で書込み又は読出し可能である。

【0033】かくしてアドレスデータ D_{A0} に基づく複数のアドレス $A_0 \sim A_{10}$ は、コマンドブロックレジスタRA及びコントロールブロックレジスタRBを構成する各レジスタ $R_1 \sim R_7$ に応じたアドレスに変換される。

【0034】メカニカル部12(図1)は、ハードディスクコントローラ9の制御のもと、複数のハードディスク(図示せず)を同軸中心上に高速回転させながら、複数の可動アーム(図示せず)の先端に取り付けられた磁気ヘッドをそれぞれハードディスクの一面又は他面に対応させて、当該各ハードディスクの両面上に対してそれぞれ映像音声データD1の書込み又は読出しを行い得るようになされている。

【0035】図3において、ハードディスクコントローラ9は、コマンドブロックレジスタRAにおけるセクタカウントレジスタ R_3 の全てのセクタカウント数とステータス/コマンドレジスタ R_5 のコマンドコードをメモ

リアドレス発生部13内のコマンドコード部13A、データ書込みカウンタ13B及びセクタカウンタ13Cに与える。

【0036】これによりコマンドコード部13Aは、セクタカウントレジスタR_sのセクタカウント数とステータス/コマンドレジスタR_cの書込みコマンドコードを判断し、書込み系コマンドであるコマンドコード（例えばWRITE SECTORS(30h)、WRITE DMA(CAh)等）の書込みを検出してメモリアドレス発生部13全体を動作可能状態に設定する。

【0037】またデータ書込みカウンタ13Bは、セクタカウントレジスタR_sのセクタカウント数とステータス/コマンドレジスタR_cに指定された各論理ブロックアドレスに応じた各論理セクタ内のデータに対応するアドレスをワード単位で順次生成する。セクタカウンタ13Cは、データ書込みカウンタ13Bにおいて先読みしたカウンタの桁上げ動作の回数を検出し、又はセクタカウントレジスタR_sの減算カウンタ動作の回数を検出して、その動作回数をセクタ単位（512〔byte〕単位）で加算してなるアドレスを順次生成する。

【0038】メモリアドレス合成部13Dは、データ書込みカウンタ13B及びセクタカウンタ13Cにおいてそれぞれカウンタアップしてなる出力を受け、これらのアドレスを加算してメモリアドレスデータD_{MA}としてメモリアドレスインタフェイス14を介して映像音声データ出力部6内の映像音声出力コントローラ15に与える。

【0039】なおメモリアドレス発生部13は、メモリアドレス合成部13Dから連続する1ブロック単位の映像音声データのメモリアドレスデータD_{MA}が映像音声出力コントローラ15に送出された後、コマンドレジスタRAへのデータ書込み状態を検出し、当該検出結果に応じてデータ書込みカウンタ13B及びセクタカウンタ13Cをクリアして再度アドレスカウントを行う。

【0040】あるいはここでMPEG2規格に基づく映像音声データにおいて、最初の数分の一部分だけにIピクチャデータと音声データとを集合させて、残りをPピクチャデータ及びBピクチャデータの順に並べ替えたディスク用可変長サイズデータの場合であつて、最初の数分の一部分だけ書き込んで読み出したい場合には、必要に応じて映像音声データ出力部6内の第1又は第2のバンクメモリ16、17を所定数のパーティションに分割した後、そのうち最初から数個目のパーティションを順次指定したメモリアドレスに書き込むことにより、連続する映像音声データD1を1画像ブロック単位内で第1又は第2のバンクメモリ16、17に書き込むようにする。

【0041】このときAVメモリパーティションカウンタ13Eは、データ書込みカウンタ13B及びセクタカウンタ13Cから得られる出力の合成結果が所定数のパ

ーティションのうち最初から数個目のパーティションのみに相当する範囲でアドレスを生成した後、クリアリセットして当該アドレス生成を停止させてハードディスクコントローラ9のデータ転送を終了する。なおこの場合、ハードディスクコントローラ9は、セクタカウントレジスタR_sの所定回数のセクタカウント数が転送終了したらクリアリセットするようにしても良い。

【0042】このようにメモリアドレス発生部13は、CPU2から送出されるアドレスデータD_{MA}に基づくアドレスに応じてハードディスクコントローラ9内の所定のレジスタR_s及びR_cを順次指定した後、当該各指定したアドレスに基づいて上述したメモリアドレスデータD_{MA}を順次ワード単位で生成した後、これを映像音声出力コントローラ15に供給する。

【0043】また映像音声データ出力部6内のレジスタセット部11は、CPU2からホストバス4及びコントローラインタフェイス部10を順次介して送出されるアドレスデータD_{MA}及びコントロールデータD_{CON}に基づいて、映像音声出力コントローラ15に対してデータ転送が可能な状態にセットされたか否かをセット状態データD_{SET}を送出する。

【0044】映像音声出力コントローラ15は、セット状態データD_{SET}がデータ転送が可能な状態であることを表すとき、順次ワード単位で供給されるメモリアドレスデータD_{MA}を第1のバンクメモリ16又は第2のバンクメモリ17に交互に送出し、第1のバンクメモリ16又は第2のバンクメモリ17をそれぞれメモリアドレスデータD_{MA}に基づくメモリアドレスに応じて順次指定する。

【0045】因みに図4（A）に示すように、本実施の形態の場合にはメモリアドレスデータD_{MA}の1回に転送できる最大の転送データ数は128〔kbyte〕である。すなわちセクタカウントレジスタR_sは8ビット幅であるため、8ビット幅のセクタカウントレジスタR_sの設定最大値は256回のセクタ転送回数の設定値となる。従つてハードディスクコントローラ9の1セクタのデータは、1ワード=2〔byte〕の256回のワードデータ転送による512〔byte〕であるため、メモリアドレスデータD_{MA}は最大128〔kbyte〕（256回×512〔byte〕）のデータサイズを設定可能な1転送ブロック単位として第1のバンクメモリ16又は第2のバンクメモリ17に転送される。なお図4（B）に示すように、1フレーム（1画像ブロック）が512〔kbyte〕からなる場合、第1のバンクメモリ16又は第2のバンクメモリ17から順次交互に繰り返し読み出される128〔kbyte〕毎の映像音声データD1が4倍集められて1画像ブロックを形成するようになされている。

【0046】これにより第1のバンクメモリ16又は第2のバンクメモリ17には、レジスタセット部11を介して供給される映像音声データD1が順次指定されたメ

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モリアドレスに対応してフレーム単位で交互に書き込まれる。このとき第1のバンクメモリ16又は第2のバンクメモリ17のうち一方のメモリに1フレーム分の映像音声データD1を書き込んでいる間に、他方のメモリから既に書き込まれた1フレーム分の映像音声データD1を読み出してデコーダ部18に送出する。

【0047】デコーダ部18は、第1のバンクメモリ16又は第1のバンクメモリ17からフレーム毎に交互に与えられる映像音声データD1をデコードした後、順次入力されたフレーム毎にAVモニタ部19に送出する。かくしてAVモニタ部19では、映像音声データD1に基づく映像及び音声が表示及び放音される。

【0048】これに対して、映像音声データ出力部6のみを単独に使い、ハードディスク5に映像音声データを書き込む制御を行わない場合には、映像音声出力コントローラ15は、レジスタセット部11から与えられるセット状態データD_{SET}がデータ転送が不可能な状態であることを表すとき、CPU2はATAハードディスクドライバ部5に対して映像音声データD1を供給することなく、CPU2がコントローラインタフェース部10及びレジスタセット部11を介して直接的に第1のバンクメモリ16又は第2のバンクメモリ17に対してワード単位で交互にメモリアドレスを順次指定して、当該指定されたメモリアドレスに対応させて映像音声データD1をフレーム毎に交互に書き込む。

【0049】この後上述の場合と同様に、第1のバンクメモリ16又は第2のバンクメモリ17からフレーム毎に交互に供給される映像音声データD1がデコーダ部18に与えられ、当該デコーダ部18においてデコードされた後、順次入力されたフレーム毎にAVモニタ部19に送出される。

【0050】(2) データ書き込み処理手順

CPU2は図5に示すようなデータ書き込み処理手順を実行することによって、データ書き込み時にATAハードディスクドライバ部5内のハードディスクコントローラ9に映像音声データD1Aを転送すると共に、当該転送した映像音声データD1をAVモニタ部19にリアルタイムで出力する。

【0051】すなわちCPU2は、まずハードディスクコントローラ9内のコントロールブロックレジスタRBのうちアルタネットステータス/デバイスコントロールレジスタR₁にデバイス選択コードを設定することにより(ステップSP1)、ATAハードディスクドライバ部5内のメカニカル部12に収納されているデバイス0、デバイス1など複数種類のデバイス選択コード設定機能を有するハードディスクドライバの中から当該デバイス選択コードに対応するハードディスクを選択する。

【0052】続いてハードディスクコントローラ9は、ステータス/コマンドレジスタR₂内のBSY(ビジービット)及びDRQ(データリクエストビット)の値

と共に「0」に設定した後、CPU2に対して入出力可能状態信号D_{IO_{RDY}}を送出する(ステップSP2)。因みにBSYは値「0」のときステータスコードの設定処理が終了したことを表し、DRQは値「0」のときステータス/コマンドレジスタR₂に対してホストCPUのデータ転送要求への対応準備ができていないことを表す。また、入出力可能状態信号D_{IO_{RDY}}は、データ読み出し信号(IOR-)、データ書き込み信号(IOW-)の発生期間中はアクティブである必要があり、またディスクドライバ内部でデータ転送が滞ったときには不活性となつてホストCPUに対してアクセスウェイト信号を論理的に発生するのに使用される。

【0053】CPU2は、ハードディスクコントローラ9内のステータス/コマンドレジスタR₂、あるいは同一内容をもつアルタネットステータスレジスタR₆をループ処理により繰返し読み出し処理を行い、書き込まれたステータスコード、BSY=0、DRQ=0を確認した後(ステップSP3)、転送予定の全てのセクタカウンタ数をセクタカウントレジスタR₃に設定すると共に(ステップSP4)、当該セクタ単位で順次論理ブロックアドレスを指定して論理ブロックアドレスレジスタR₄に設定する(ステップSP5)。これによりコマンドブロックレジスタRA及びコントロールブロックレジスタRBは書き込み動作状態に設定される。

【0054】続いてCPU2は、ステータス/コマンドレジスタR₂に書き込みコマンドコードを書き込むことにより、コマンドブロックレジスタRA及びコントロールブロックレジスタRBの各レジスタの値を設定した後(ステップSP6)、所定時間(例えばATA標準規格では400[ns])経過させて当該各レジスタの値を安定させる(ステップSP7)。これと共にハードディスクコントローラ9は、ステータス/コマンドレジスタR₂に書き込まれた書き込みコマンドコードを検出することにより、メモリアドレス発生部13を動作可能状態に設定する。

【0055】続いてハードディスクコントローラ9は、ステータス/コマンドレジスタR₂内のBSYの値を「0」及びDRQの値を共に「1」に設定した後、CPU2に対して入出力可能状態信号D_{IO_{RDY}}を送出する(ステップSP9)。CPU2は、ハードディスクコントローラ9内のステータス/コマンドレジスタR₂、あるいは同一内容をもつアルタネットステータスレジスタR₆をループ処理により繰返し読み出し処理を行い、レジスタに書き込まれたステータスコードをBSY=0かつDRQ=1となるまで繰返し読み出す(ステップSP10)。

【0056】この後CPU2は、ハードディスクコントローラ9に対してデータの転送を開始し、まずハードディスクコントローラ9に1セクタ単位で映像音声データD1を転送する(ステップSP11)。ハードディスクコントローラ9は、セクタカウンタレジスタR₃のセク

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タカウント数とステータス/コマンドレジスタR_iの、コマンドコードに基づいて、1セクタのメモリアドレスデータD_{MA}を発生することにより(ステップSP12)、映像音声出力データ部6はメモリアドレスデータD_{MA}に基づいてCPU2から供給される映像音声データD1の書込みを開始する(ステップSP13)。

【0057】ハードディスクコントローラ9は、CPU2から1セクタ分の映像音声データD1が供給され終わったことを確認すると、割込み処理要求信号D_{INTRQ}を発生してCPU2に送出する(ステップSP14)。

【0058】CPU2は割込み処理要求信号D_{INTRQ}に基づいて、ハードディスクコントローラ9内のステータス/コマンドレジスタR_iに書き込まれた次のセクタに対応するステータスコードを読み出す(ステップSP15)。これに応じてハードディスクコントローラ9が割込み処理要求信号D_{INTRQ}をクリアしたことを確認すると(ステップSP14)、ステップSP11~SP13と同様のデータ書込み処理を行う。このようにCPU2は、順次セクタ毎にデータ転送を行うと共に、ハードディスクコントローラ9は映像音声出力データ部6にセクタ単位でメモリアドレスデータD_{MA}を送出し続ける。

【0059】ハードディスクコントローラ9は、セクタカウントレジスタR_iに基づいて全セクタカウント数が終了したと判断したとき、ステータス/コマンドレジスタR_i内のBSY及びDRQの値を共に「0」に設定する(ステップSP30)。これによりハードディスクコントローラ9はメモリアドレスデータD_{MA}の発生を停止して、映像音声出力データ部6は映像音声データD1の書込みを終了する(ステップSP31)。これと共にハードディスクコントローラ9は、割込み処理要求信号D_{INTRQ}を発生して(ステップSP31)、これをCPU2に送出する(ステップSP32)。

【0060】CPU2は割込み処理要求信号D_{INTRQ}を受けると、全データの転送終了を確認するためにハードディスクコントローラ9内のステータス/コマンドレジスタR_iに書き込まれたステータスコードの読み出しを行う(ステップSP33)。これと共にハードディスクコントローラ9は、割込み処理要求信号D_{INTRQ}をクリアすることにより当該データ書込み処理手順を終了する。

【0061】(3)本実施の形態の動作及び効果
以上の構成において、このハードディスク装置1では、CPU2はATAハードディスクドライブ部5におけるハードディスクコントローラ9内の各レジスタに対してアドレスデータD_{MA}に応じたアドレスを指定すると共に、当該指定したアドレスに対応して映像音声データ生成部3から供給される映像音声データD1を書き込む。

【0062】このときハードディスクコントローラ9は、各レジスタRA、RBに応じたアドレスデータD_{MA}をメモリアドレス発生部13にワード単位で供給する

と、メモリアドレス発生部13は、当該アドレスデータD_{MA}に基づいて第1及び第2のバンクメモリ16、17に応じたメモリアドレスデータD_{MA}をワード単位で順次生成する。

【0063】このように各レジスタRA、RBに応じたアドレスデータD_{MA}を第1及び第2のバンクメモリ16、17に応じたメモリアドレスデータD_{MA}に変換するのは、ハードディスクコントローラ9内の各レジスタRA、RBには、同一アドレス位置に映像音声データD1をセクタ単位で繰り返して書き込むのに対して、映像音声データ出力部6内の第1のバンクメモリ16又は第2のバンクメモリ17には、順次累積加算されて増加したアドレス位置に映像音声データD1をワード単位で書き込むからである。

【0064】メモリアドレス発生部13は、映像音声データ出力部6内の第1のバンクメモリ16又は第2のバンクメモリ17に対して交互にワード単位のメモリアドレスデータD_{MA}を送出する。これにより第1のバンクメモリ16又は第2のバンクメモリ17は、交互にメモリアドレスデータD_{MA}に応じたアドレスが指定されると共にフレーム単位で映像音声データD1が書き込まれる。

【0065】これによりCPUはハードディスクコントローラ9に対して映像音声データD1をデータ転送する際、当該データ転送のタイミングに同期して映像音声出力データ部6の第1のバンクメモリ16又は第2のバンクメモリ17に対してデータ転送することができる。

【0066】さらに第1のバンクメモリ16又は第2のバンクメモリ17のうち一方のメモリにフレーム単位でデータを書き込むと共に他方のメモリからフレーム単位でデータを読み出してAVモニタ部19に送出する動作を交互に繰り返すようにしたことにより、ディスクドライブに対する書込み処理とリアルタイムで映像音声データをモニタ表示することができる。

【0067】以上の構成によれば、このハードディスク装置1では、CPU2はハードディスクコントローラ9内の各レジスタRA、RBに対してアドレスデータD_{MA}に応じたアドレスを指定した後、当該アドレスに基づいて映像音声データ出力部6内の第1のバンクメモリ16及び第2のバンクメモリ17に対応するアドレスを生成し、当該生成されたアドレスを交互に指定して、第1のバンクメモリ16又は第2のバンクメモリ17のうち一方に映像音声データD1をフレーム単位で書き込むと共に、他方から映像音声データD1をフレーム単位で読み出してAVモニタ部19に画面表示するようにしたことにより、映像音声データD1をメカニカル部12内のハードディスクに書き込むタイミングに同期して、当該書き込んだ映像音声データD1をリアルタイムでAVモニタ部19に表示することができ、かくして転送レートを格段と向上し得るハードディスク装置1を実現することができる。

【0068】(4)他の実施の形態

なお上述の実施の形態においては、第2の記憶制御手段としての映像音声データ出力部6内の第1及び第2のバンクメモリ16、17に対して128[kbyte]毎にアドレス指定してデータ転送するようにした場合について述べたが、本発明はこれに限らず、第1及び第2のバンクメモリ16、17がそれぞれ所定数のパーティションに区切られており、当該各パーティションに順次メモリアドレスを指定して繰り返し書き込むようにしても良い。

【0069】例えば図6(A)に示すように16[kbyte]毎にアドレス指定してデータ転送する場合、第1又は第2のバンクメモリ16、17から読み出される16[kbyte]毎の映像音声データD1を所定数に分割して転送することにより1画像ブロックを形成することができる(図6(B))。またこの場合、メモリアドレス発生部13から出力されるメモリアドレスデータD_{MA}に必要とされるアドレスビット数を14ビット(図面に実施の形態では19ビット)に減らすことができる。

【0070】また上述の実施の形態においては、ハードディスク装置1によつて映像音声データD1をハードディスクに書き込むと共に、表示手段としてのAVモニタ部19に出力して画面表示する場合について述べたが、本発明はこれに限らず、映像音声データD1をハードディスクから読み出す場合についても本発明は適用することができる。

【0071】この場合、図5との対応部分に同一符号を付した図7に示すデータ読出し処理手順において、上述したステップSP7に続いて、ハードディスクコントローラは、ステータス/コマンドレジスタR、内のBSYの値を「0」及びDRQの値を共に「1」に設定した後(ステップSP9)、CPU2に対して割込み処理要求信号D_{INTRQ}を発生する(ステップSP40)。CPU2は割込み処理要求信号D_{INTRQ}を受けると、ハードディスクコントローラ9内のステータス/コマンドレジスタR、に書き込まれたステータスコードを読み出す(ステップSP41)。

【0072】この後ハードディスクコントローラ9は割込み処理要求信号D_{INTRQ}をクリアしたことを確認すると(ステップSP40)、CPU2はハードディスクコントローラ9に対してデータの転送を開始し、ハードディスクコントローラ9に1セクタ単位で映像音声データD1を転送する(ステップSP42)。ハードディスクコントローラ9は、セクタカウンタレジスタR、のセクタカウント数とステータス/コマンドレジスタR、のコマンドコードに基づいて、1セクタのメモリアドレスデータD_{MA}を発生することにより(ステップSP43)、映像音声出力データ部6はメモリアドレスデータD_{MA}に基づいてCPU2から供給される映像音声データD1の書き込みを開始する(ステップSP44)。

【0073】ハードディスクコントローラ9は、CPU

2から1セクタ分の映像音声データD1が供給され終わったことを確認すると、割込み処理要求信号D_{INTRQ}を発生してCPU2に送出する(ステップSP45)。CPU2は割込み処理要求信号D_{INTRQ}に基づいて、ハードディスクコントローラ9内のステータス/コマンドレジスタR、に書き込まれた次のセクタに対応するステータスコードを読み出す(ステップSP46)。これに応じてハードディスクコントローラ9が割込み処理要求信号D_{INTRQ}をクリアしたことを確認すると(ステップSP45)、ステップSP42〜SP44と同様のデータ書き込み処理を行う。このようにCPU2は、順次セクタ毎にデータ転送を行うと共に、ハードディスクコントローラ9は映像音声出力データ部6にセクタ単位でメモリアドレスデータD_{MA}を送出し続ける。

【0074】ハードディスクコントローラ9は、セクタカウンタレジスタR、に基づいて全セクタカウント数が終了したと判断したとき、ステータス/コマンドレジスタR、内のBSY及びDRQの値を共に「0」に設定し(ステップSP60)、同じく全データ転送完了したと判断する。CPU2はステータス/コマンドレジスタR5を読み出す(ステップSP61)。これと共にハードディスクコントローラ9は、メモリアドレスデータの発生を停止して、映像音声出力データ部6は映像音声データD1の書き込みを終了すると共に(ステップSP62)、ハードディスクコントローラ9は当該データ読出し処理手順を終了する。

【0075】このようにデータ読出し処理手順を実行することにより、ハードディスク装置1によつて映像音声データD1をハードディスクから読み出すと共に、AVモニタ部19に出力して画面表示することができる。

【0076】さらに上述の実施の形態においては、各セクタ転送毎に割込み処理要求信号D_{INTRQ}の発生するPIO(プログラムI/O)転送について述べたが、本発明はこれに限らず、ATA/ATAPI標準に記載のDMA転送、Ultra DMA転送、さらにATA/ATAPI標準方式の将来の拡張方式にも適用することができる。

【0077】さらに上述の実施の形態においては、第1の記憶制御手段としてのハードディスクコントローラ9とアドレス生成手段としてのメモリアドレス発生部13とを別体に設けた場合について述べたが、本発明はこれに限らず、ハードディスクコントローラ9及びメモリアドレス発生部13を一体に設けるようにしても良い。

【0078】さらに上述の実施の形態においては、映像音声データD1を書き込む記録媒体としてハードディスクを適用した場合について述べたが、本発明はこれに限らず、その他CD-ROMや磁気テープ等の種々のデバイスに広く適用することができる。すなわちデータ処理装置としてハードディスク装置1以外の他の装置を適用し得る。

【0079】

【発明の効果】上述のように本発明によれば、外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1のステップと、第1の記憶手段に指定された第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成する第2のステップと、第2の記憶手段に第2のアドレスを指定して映像データをフレーム毎に記憶する第3のステップと、記録媒体に書き込むタイミングに同期して、第2の記憶手段から映像データをフレーム毎に読み出して画面表示する第4のステップとを設けたことにより、映像データをフレーム毎に記録媒体に書き込むタイミングに同期して、当該書き込んだ映像データをフレーム毎にリアルタイムで画面表示することができ、かくして転送レートを格段と向上し得るデータ処理方法を実現することができる。

【0080】また本発明においては、外部から供給される映像データを第1の記憶手段に順次第1のアドレスを指定してフレーム毎に記憶する第1の記憶制御手段と、第1の記憶制御手段によつて指定された第1のアドレスに基づいて第2の記憶手段に対応する第2のアドレスを生成するアドレス生成手段と、第2の記憶手段にアドレス生成手段によつて生成された第2のアドレスを指定して映像データをフレーム毎に記憶する第2の記憶制御手段と、第1の記憶手段から映像データをフレーム毎に読み出して記録媒体に書き込む書込手段と、書込手段が記録媒体に書き込むタイミングに同期して、第2の記憶手段から映像データをフレーム毎に読み出して画面表示する表示手段とを設けたことにより、映像データをフレーム毎に記録媒体に書き込むタイミングに同期して、当該書き込んだ映像データをフレーム毎にリアルタイムで画面表示することができ、かくして転送レートを格段と向*

* 上し得るデータ処理装置を実現することができる。

【図面の簡単な説明】

【図1】本発明によるハードディスク装置の構成の一実施の形態を示すブロック図である。

【図2】本発明によるATAインタフェース部によるアドレス変換処理の説明に供する図表である。

【図3】本発明によるハードディスクコントローラ及びメモリアドレス発生部の内部構成を示すブロック図である。

10 【図4】本実施の形態による各バンクメモリへの書込み状態を示す略線図である。

【図5】本実施の形態によるデータ書込み処理手順を示すタイミングチャートである。

【図6】他の実施の形態による各バンクメモリへの書込み状態を示す略線図である。

【図7】他の実施の形態によるデータ読出し処理手順を示すタイミングチャートである。

【符号の説明】

1……ハードディスク装置、2……CPU、3……映像音声データ生成部、4A……アドレスバス、4B……データバス、4C……コントロールバス、5……ATAハードディスクドライブ部、6……映像音声データ出力部、7……ATAインタフェース部、9……ハードディスクコントローラ、10……コントローラインタフェース部、11……レジスタセット部、12……メカニカル部、13……メモリアドレス発生部、15……映像音声出力コントローラ、16……第1のバンクメモリ、17……第2のバンクメモリ、18……デコーダ部、19……A.Vモニタ部、RA……コマンドブロックレジスタ、RB……コントロールブロックレジスタ、D1……映像音声データ、DA……アドレスデータ、DMA……メモリアドレスデータ。

【図2】

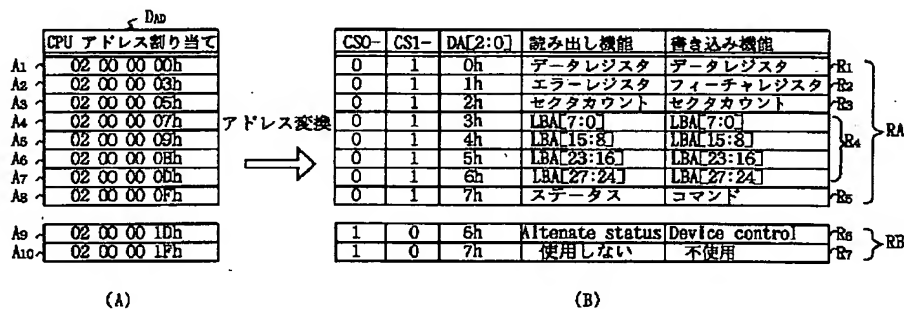


図2 ATAインタフェース部によるアドレス変換処理

【図1】

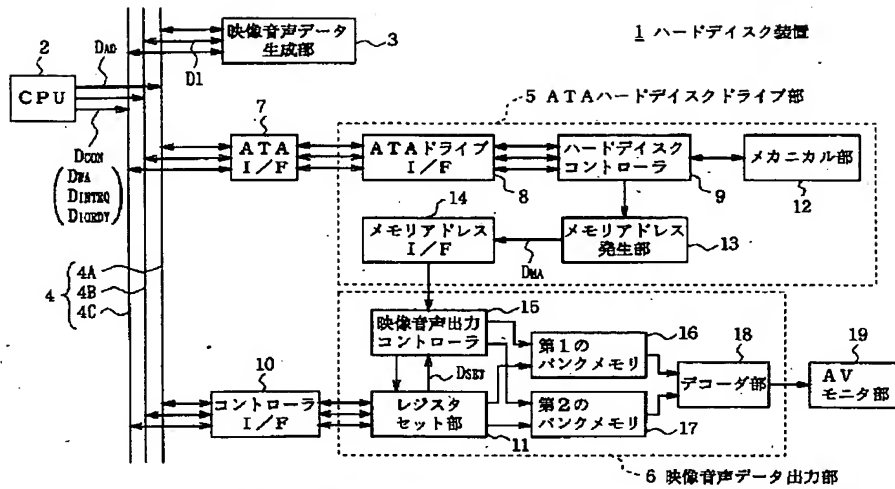


図1 本実施の形態によるハードディスク装置の構成

【図3】

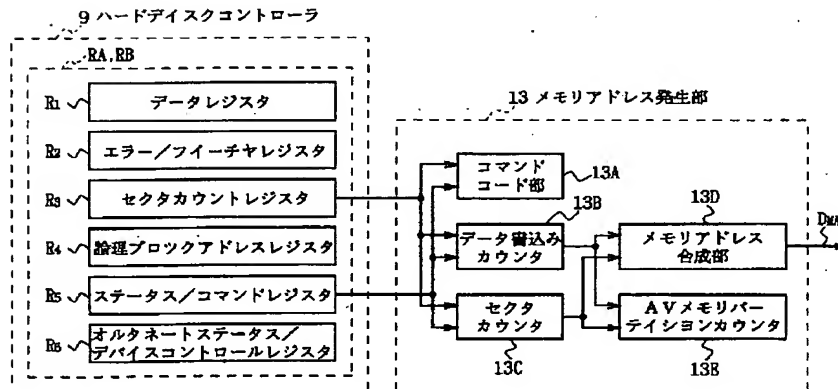


図3 ハードディスクコントローラ及びメモリアドレス発生部の内部構成

【図6】

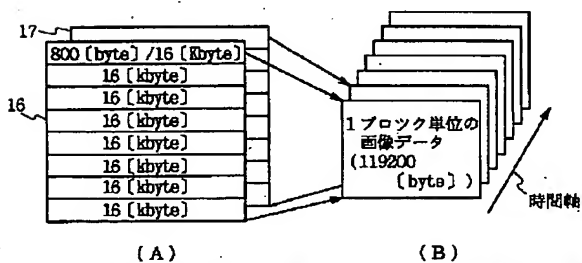


図6 他の実施の形態による各バンクメモリへの書き込み状態

〔図4〕

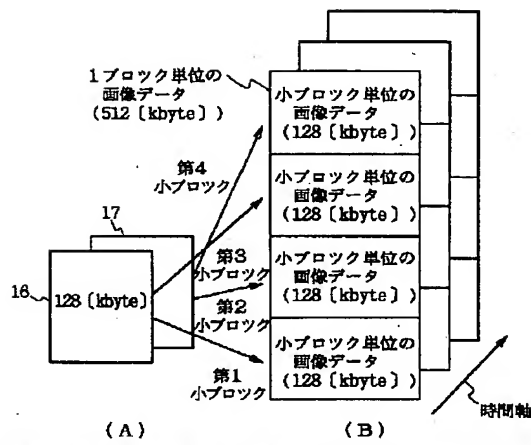


図4 本実施の形態による各バンクメモリへの書き込み状態

〔図5〕

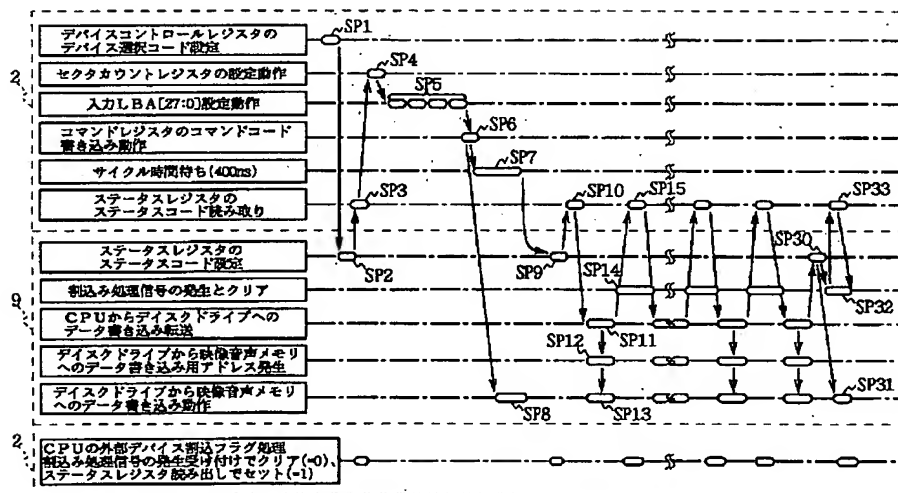


図5 本実施の形態によるデータ書き込み処理手順

【図7】

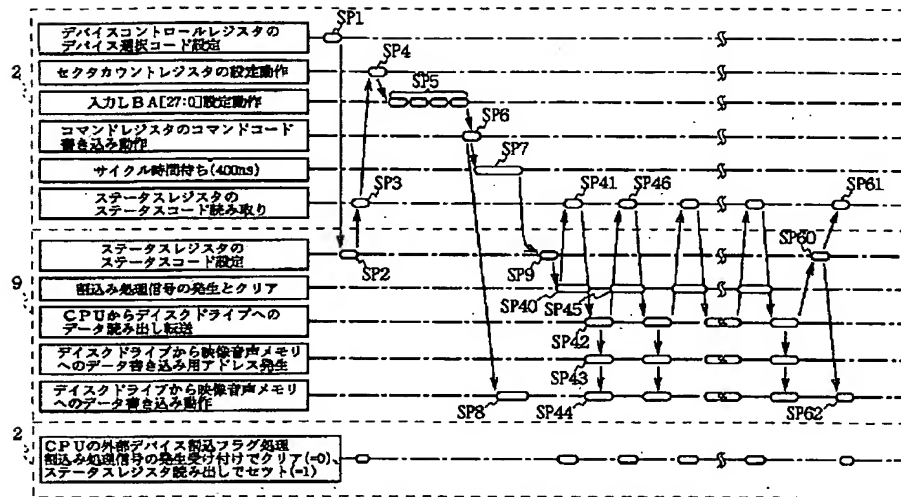


図7 他の実施の形態によるデータ読み出し処理手順

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-187342

(43)Date of publication of application : 09.07.1999

(51)Int.Cl.

H04N 5/78

G11B 20/10

H04N 5/92

(21)Application number : 09-351569

(71)Applicant : SONY CORP

(22)Date of filing : 19.12.1997

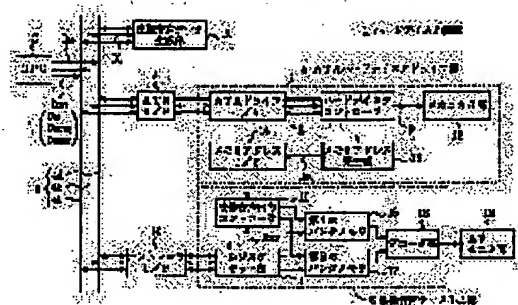
(72)Inventor : OKADA SHUNJI

(54) DATA PROCESSING METHOD AND DATA PROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To improve a transfer rate by designating a first address in a first storage means to store transmitted video data for every frame, designating the second address based on the first address to store video data for every frame and reading video data from the second storage means for every frame by means of the synchronization with a writing timing to display it.

SOLUTION: CPU 2 designates the address corresponding to address data DAD and, after that, generates the addresses corresponding to a first bank memory and the second bank memory 17 in a video voice data output part 6 based on the address. The generated addresses are alternately designated, audiovideo data D1 is written in one of the first bank memory 16 of the second one 17 by frame unit, audiovideo data D1 is read from the other one by frame unit and it is displayed on the screen of an AV monitor part 19. Thus, screen display is enabled by synchronizing with the timing by which audiovideo data D1 is written on a hard disk.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

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2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The 1st step which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside, The 2nd step which generates the 2nd address corresponding to the 2nd storage means based on the 1st address of the above specified as the storage means of the above 1st, The 3rd step which specifies the 2nd address of the above as the storage means of the above 2nd, and memorizes the above-mentioned image data for every above-mentioned frame, The data-processing approach characterized by having the 4th step which reads and carries out a screen display of the above-mentioned image data for every above-mentioned frame from the storage means of the above 2nd synchronizing with the timing written in the above-mentioned record medium.

[Claim 2] At the 2nd step of the above, the storage means of the above 2nd has the 1st and 2nd bank memory. At the above 3rd and the 4th step While specifying the 2nd address of the above as the 1st or 2nd bank memory of the above by turns and memorizing the above-mentioned image data for every above-mentioned frame to one side among the 1st or 2nd bank memory of the above The data-processing approach according to claim 1 characterized by reading and carrying out a screen display of the above-mentioned image data for every above-mentioned frame from another side.

[Claim 3] The 1st storage control means which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside, An address-generation means to generate the 2nd address corresponding to the 2nd storage means based on the 1st address of the above therefore specified as the storage control means of the above 1st, The 2nd storage control means which specifies the 2nd address of the above therefore generated at the above-mentioned address-generation means as the storage means of the above 2nd, and memorizes the above-mentioned image data for every above-mentioned frame, The write-in means which reads the above-mentioned image data from the storage means of the above 1st for every above-mentioned frame, and is written in a record medium, The data processor characterized by having a display means by which the above-mentioned write-in means reads and carries out a screen display of the above-mentioned image data for every above-mentioned frame from the storage means of the above 2nd synchronizing with the timing written in the above-mentioned record medium.

[Claim 4] The storage means of the above 2nd has the 1st and 2nd bank memory. The storage control means of the above 2nd While specifying by turns the 2nd address of the above therefore generated by the above-mentioned address-generation means as the 1st or 2nd bank memory of the above and writing the above-mentioned image data in one side for every above-mentioned frame among the 1st or 2nd bank memory of the above The data processor according to claim 3 characterized by what the above-mentioned image data are read from another side for every above-mentioned frame, and is displayed on the above-mentioned display means.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Table of Contents] This invention is explained in order of the following.

[0002] The whole gestalt (1) hard disk drive unit configuration of operation of technical-problem The means for solving a technical problem invention which technical field Prior-art invention to which invention belongs tends to solve (drawing 1 - drawing 4)

(2) Data write-in procedure (drawing 5)

(3) Actuation of the gestalt of this operation, and the gestalt of operation of others [effectiveness / (4)] (drawing 6 - drawing 7)

Effect of the invention [0003]

[Field of the Invention] This invention is applied to the hard disk drive unit which performs the writing and read-out of image voice data, concerning the data-processing approach and a data processor, and is suitable.

[0004]

[Description of the Prior Art] the whole surface or the thing which boiled on the other hand, carries out the data compression of the image voice data by making it correspond if needed, respectively on both sides of each hard disk concerned, and was recorded of a hard disk is used, respectively in the magnetic head attached at the tip of two or more movable arms, carrying out high-speed rotation of two or more hard disks on a coaxial core as this kind of a hard disk drive unit conventionally.

[0005] A track is formed in both sides of each [these] hard disk concentric circular, respectively, and ** or an intermediary track number is assigned to the most inner circumference from the outermost periphery. Furthermore, each track is divided into the sector which makes a predetermined data length a unit, and the logic block address (LBA) as a sector number is assigned to each sector concerned.

[0006] In this hard disk drive unit, CPU sets the sector number of counts showing the count of a sector transfer of each sector concerned as a data register while specifying the data register prepared in the disk drive according to the logic block address assigned for every sector of a predetermined hard disk.

[0007] Then, CPU is made as [write / for every frame / image voice data], carrying out sequential addressing of a series of image voice data which consists of two or more sectors to the data register in a disk drive, after writing each data block in each buffer memory of a bank-switching method in order of FIFO (First In First Out) by turns one by one for every [for every 1 image voice data block] frame.

[0008] Then, CPU is made as [output / to the monitoring device by which read from the memory concerned and external connection was made if needed], after writing in for every frame, carrying out sequential addressing of the image voice data read from buffer memory to the memory in which it was built by the image voice output circuit.

[0009]

[Problem(s) to be Solved by the Invention] By the way, CPU is **** in ****, if image voice data is not transmitted per frame, respectively, carrying out sequential assignment of the address which cannot specify [as opposed to / when carrying out data transfer of a series of image voice data stored in buffer

memory to both a disk drive and an image voice output circuit at coincidence / the data register in a disk drive, and the memory in an image voice output circuit] the same address directly, but is mutually different.

[0010] Moreover, for CPU, the processing time when setting up various registers other than the data register in the disk drive concerned before starting data transfer to a disk drive, until the set point of the register concerned is decided is about 100-300 each time. It was once in every [ns]. Furthermore, when data interruption was processed two or more times after CPU ended data transfer to the disk drive, it required once the processing time before and behind about 5-10 [mus] for whenever [the].

[0011] For this reason, when data transfer of a series of image voice data was carried out continuously, in consideration of a register setup and interrupt processing which were mentioned above being performed, it was made as [make / the image voice data concerned / transmit for every frame unit within predetermined time amount (for example, 128 [kbyte] less than 33 [ms] and another example 512 [kbyte] less than 0.5 [ms])].

[0012] Therefore, when data transfer is made to once start to a disk drive, CPU is **** in ****, if image voice data must be transmitted to a data register for every frame unit and image voice data of each frame unit is not transmitted to memory to an image voice output circuit next, without stopping on the way. Consequently, the problem of taking the data transfer time to a disk drive and an image voice data output circuit for a long time, respectively is *****.

[0013] In case data transfer of the CPU is carried out to a disk drive, furthermore, within a disk drive Retry (rewrite) actuation, When transfer operation, such as a jump between tracks on a hard disk or a jump between sectors, etc. is performed, Condition signal DIORDY at the time of performing data transfer from a disk drive at the time of each actuation concerned which can be outputted and inputted Use and the signal is stopped temporarily, The waiting demand signal for access for keeping the access processing from CPU waiting temporarily indicated by the ATA standard method is emitted. These above results, CPU is **** in ****, if it carries out with a data transfer rate more nearly high-speed than the usual data transfer rate and data transfer which continued by another processing in another side and an image voice output circuit is not performed in a hard disk, in order to perform discontinuous data transfer in time to a disk drive and to perform a real-time operation for this reason.

[0014] For this, the problem of being hard to judge on real time whether data transfer [as opposed to / the data transfer to a disk drive will be processed not by real time but by another time amount, and / a disk drive in CPU] having been performed certainly is *****.

[0015] This invention was made in consideration of the above point, and tends to propose the data-processing approach and data processor which may improve a transfer rate markedly.

[0016]

[Means for Solving the Problem] In order to solve this technical problem, it sets to this invention. The 1st step which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside, The 2nd step which generates the 2nd address corresponding to the 2nd storage means based on the 1st address specified as the 1st storage means, The 3rd step which specifies the 2nd address as the 2nd storage means, and memorizes image data for every frame, and the 4th step which reads and carries out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium were prepared.

[0017] Consequently, synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame.

[0018] Moreover, the 1st storage control means which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied from the outside for every frame in this invention, An address-generation means to generate the 2nd address corresponding to the 2nd storage means based on the 1st address therefore specified as the 1st storage control means, The 2nd storage control means which specifies the 2nd address therefore generated at the address-generation means as the 2nd storage means, and memorizes image data for every frame, The write-in means which reads image data from the 1st storage means for every frame, and is written in a record medium, and a display means by which a

write-in means read and carried out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium were established.

[0019] Consequently, synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame.

[0020]

[Embodiment of the Invention] About a drawing, the gestalt of 1 operation of this invention is explained in full detail below.

[0021] (1) In the whole hard disk drive unit block diagram 1, 1 shows the hard disk drive unit which consists of a standard ATA (AT attachment) method of an IDE (intelligent drive electronics) interface as a whole, and is made as [carry out / , respectively / through the host bus 4 / at the ATA hard disk drive section 5 and the image voice data output section 6 / to CPU2 / data transfer of the image voice data D1 by which sequential supply is therefore carried out from the image voice data generation section 3].

[0022] The ATA interface section 7 is formed between the host bus 4 and the ATA hard disk drive section 5, and it is made as [give / through the ATA drive interface section 8 in the ATA hard disk drive section 5 / the various data supplied from CPU2 and the image voice data generation section 3 / the hard disk controller 9].

[0023] Moreover, the controller interface section 10 is formed between the host bus 4 and the image voice data output section 6, and it is made as [give / the various data supplied from CPU2 and the image voice data generation section 3 / the register set section 11 in the image voice data output section 6].

[0024] This host bus 4 consists of address bus 4A, data bus 4B, and control bus 4C. Among these, address bus 4A is a bus for giving the address data DAD for specifying the address of the various registers sent out from CPU2 to the ATA interface section 7 and the controller interface section 10.

[0025] Moreover, data bus 4B is a bus for giving the image voice data D1 supplied from the image voice data generation section 3 to the ATA interface section 7 and the controller interface section 10.

[0026] Furthermore, control bus 4C is CDC DCON for controlling the data transfer to each register in the ATA hard disk drive section 5 sent out from CPU2. While giving the ATA interface section 7, when the timing of the data transfer concerned becomes discontinuous, in order that the ATA hard disk drive section 5 may suspend data transfer temporarily, it is a bus for sending out the weight signal DWA to CPU2. In addition, this control bus 4C is the ATA hard disk drive section 5 concerned to the interrupt-processing demand signal DINTRQ, when the data transfer to each register in the ATA hard disk drive section 5 is completed. While sending out to CPU2, when it is in a condition accessible in the case of the data transfer concerned, it is the condition signal DIORDY which can be outputted and inputted from the ATA interface section 7 and the controller interface section 10. It is also a bus for sending out to CPU2.

[0027] The hard disk controller 9 in the ATA hard disk drive section 5 has the command block register RA and the control block register RB, and specifies them here according to the address assigned based on the address data DAD to which each registers RA and RB concerned were supplied from CPU2 for every sector of the predetermined hard disk in the mechanical section 12 (not shown).

[0028] At this time, the ATA interface section 7 is made as [specify / to the command block register RA and the control block register RB in the hard disk controller 9 / the address according to address data DAD] by performing predetermined address translation processing to the address data DAD supplied through address bus 4A from CPU2.

[0029] Specifically, address data DAD consist of two or more address A0 -A10 expressed with 32 bits of a hexadecimal notation, respectively, as shown in drawing 2 (A). Address A1 -A10 of these plurality are changed into the address corresponding to the command block register RA and the control block register RB through the ATA interface section 7.

[0030] The address after conversion is shown in drawing 2 (B), and, therefore, it is expressed 1-bit "CS0 -" and "CS1 -" to "DA (device address)" of a triplet, among these "CS0 -" and "CS1 -" are the addresses for choosing the register which both serves as a candidate for a setting out of two or more registers. Address A1 -A8 among two or more address A1 -A10 actually based on address data DAD "CS0 -" is a

value "0", and "CS1 -" expresses a value "1", and the command block register RA is chosen at this time. Moreover, address A9 And "CS0 -" is a value "1", and, as for A10, "CS1 -" expresses a value "0", and the control block register RB is chosen at this time.

[0031] Moreover, "DA" shows eight kinds of device addresses from "0h" to "7h" expressed with the triplet of a hexadecimal notation, and the class of each register which constitutes the command block register RA or the control block register RB corresponding to these device addresses is chosen.

[0032] In this command block register RA, they are a data register R1, the error / feature register R2, the sector count register R3, and the logic block-address register R4. And the status / command register R5 It is and they are the alternate status / device control register R6 in the control block register RB. And non-used register R7 It is. Data register R1 It is other register R2 -R7 to writing or read-out being possible at a word unit. Writing or read-out is possible per cutting tool register.

[0033] two or more address A0 -A10 based on address data DAD in this way constitute the command block register RA and the control block register RB -- each -- register R1 -R7 It is changed into the address to which it responded.

[0034] the magnetic head attached at the tip of two or more movable arms (not shown) while the mechanical section 12 (drawing 1) carried out high-speed rotation of the basis of control of the hard disk controller 9, and two or more hard disks (not shown) on the coaxial core -- respectively -- the whole surface of a hard disk -- or on the other hand, it be alike, and it be made to correspond and be made as [perform /, respectively / to both sides top of each hard disk concerned / the writing or read-out of the image voice data D1].

[0035] It is the sector count register [in / on drawing 3 and / in the hard disk controller 9 / the command block register RA] R3. All the sector numbers of counts, and the status/command register R5 Command code is given to command code section 13A in the memory address generating section 13, data write-in counter 13B, and sector counter 13C.

[0036] Thereby, command code section 13A is the sector count register R3. The sector number of counts, and the status/command register R5 Write-in command code is judged, the writing of the command codes (for example, WRITE SECTORS (30h), WRITE DMA (CAh), etc.) which are write-in system commands is detected, and the memory address generating section 13 whole is set as the condition which can be operated.

[0037] Moreover, data write-in counter 13B is the sector count register R3. The sector number of counts, and the status/command register R5 Sequential generation of the address corresponding to the data in each logical sector according to each specified logic block address is carried out by the word unit. Sector counter 13C detects the count of carry actuation of the counter predicted in data write-in counter 13B, or is the sector count register R3. The count of subtraction count actuation is detected and sequential generation of the address which comes to add the count of actuation per sector (512 [byte] units) is carried out.

[0038] Memory address composition section 13D undergoes the output which it comes to count up in data write-in counter 13B and sector counter 13C, respectively, adds these addresses, and gives them to the image voice output controller 15 in the image voice data output section 6 through the memory address interface 14 as memory address data DMA.

[0039] In addition, after the memory address data DMA of the image voice data of the 1-block unit which continues from memory address composition section 13D are send out to the image voice output controller 15, the memory address generating section 13 detects the data write-in condition to a command register RA, clears data write-in counter 13B and sector counter 13C according to the detection result concerned, and performs an address count again.

[0040] Or in the image voice data based on MPEG 2 specification, I picture data and voice data are gathered to a part of several minutes of the beginning here. To write in and read ***** and a part of several minutes of the beginning for the remainder in the case of variable-length size data for disks rearranged in order of P picture data and B picture data By writing the partition of an eye in the memory address which carried out sequential assignment partly from the beginning, after dividing the 1st or 2nd bank memory 16 and 17 in the image voice data output section 6 into the partition of a predetermined

number if needed The continuous image voice data D1 is written in the 1st or 2nd bank memory 16 and 17 within 1 image block unit.

[0041] At this time, after the synthetic result of the output obtained from data write-in counter 13B and sector counter 13C generates the address in the range which is partly equivalent only to the partition of an eye from the beginning among the partitions of a predetermined number, clear reset of the AV memory partition counter 13E is carried out, it stops the address generation concerned, and ends the data transfer of the hard disk controller 9. In addition, the hard disk controller 9 is the sector count register R3 in this case. When the sector number of counts of the count of predetermined carries out transfer termination, it may be made to carry out clear reset.

[0042] Thus, the memory address generating section 13 responds to the address based on the address data DAD sent out from CPU2, and is the predetermined register R3 in the hard disk controller 9. And R5 After generating the memory address data DMA mentioned above based on the specified each address concerned after carrying out sequential assignment by the word unit one by one, this is supplied to the image voice output controller 15.

[0043] Moreover, the register set section 11 in the image voice data output section 6 is the address data DAD and CDC DCON which are sent out through the host bus 4 and the controller interface section 10 one by one from CPU2. It is [whether it was based and was set to the condition in which data transfer is possible to the image voice output controller 15, and] the set condition data DSET. It sends out.

[0044] The image voice output controller 15 is the set condition data DSET. When it expresses that it is in the condition in which data transfer is possible, the memory address data DMA supplied by the word unit one by one are sent out to the 1st bank memory 16 or 2nd bank memory 17 by turns, and sequential assignment of the 1st bank memory 16 or 2nd bank memory 17 is carried out according to the memory address based on the memory address data DMA, respectively.

[0045] The maximum number of transfer data which can be transmitted at 1 time of the memory address data DMA in the case of the gestalt of this operation as incidentally shown in drawing 4 (A) It is 128 [kbyte]. Namely, sector count register R3 Since it is 8-bit width of face, it is the sector count register R3 of 8-bit width of face. Setting maximum is 256. It becomes the set point of the count of a sector transfer of a time. Therefore, the data of 1 sector of the hard disk controller 9 are based on 256 WORD data transfer of 1 word =2[byte]. Since it is 512 [byte], the memory address data DMA are max. It considers as 1 transfer block unit which can set up the data size of 128 [kbyte] (256 time x 512[byte]), and is transmitted to the 1st bank memory 16 or 2nd bank memory 17. In addition, as shown in drawing 4 (B), it is one frame (1 image block). When consisting of 512 [kbyte], it is repeatedly read from the 1st bank memory 16 or 2nd bank memory 17 by turns one by one. It is made as [form / the image voice data D1 of every 128[kbyte] is collected 4 times, and / 1 image block].

[0046] Thereby, the image voice data D1 supplied through the register set section 11 is written in the 1st bank memory 16 or 2nd bank memory 17 by turns per frame corresponding to the memory address by which sequential assignment was carried out. While writing the image voice data D1 for one frame in one memory among the 1st bank memory 16 or the 2nd bank memory 17 at this time, the image voice data D1 for one already written-in frame is read from the memory of another side, and it sends out to the decoder section 18.

[0047] After the decoder section 18 decodes the image voice data D1 given by turns for every frame from the 1st bank memory 16 or 1st bank memory 17, it is sent out to AV monitor section 19 for every frame by which the sequential input was carried out. the image and voice based on [in this way] the image voice data D1 at AV monitor section 19 -- a display -- and sound emission is carried out.

[0048] on the other hand, in not performing control which uses only the image voice data output section 6 independently, and writes image voice data in a hard disk 5 The image voice output controller 15 is the set condition data DSET given from the register set section 11. When it expresses that it is in the condition in which data transfer is impossible, CPU2, without supplying the image voice data D1 to the ATA hard disk drive section 5 CPU2 carries out sequential assignment of the memory address by turns by the word unit to the 1st bank memory 16 or 2nd bank memory 17 through the controller interface section 10 and the register set section 11 directly. It is made to correspond to the specified memory

address concerned, and the image voice data D1 is written in by turns for every frame.

[0049] After the image voice data D1 supplied by turns for every frame is given to the decoder section 18 and decoded in the decoder section 18 concerned like the next above-mentioned case from the 1st bank memory 16 or 2nd bank memory 17, it is sent out to AV monitor section 19 for every frame by which the sequential input was carried out.

[0050] (2) Therefore, the data write-in procedure CPU 2 outputs the transmitted image voice data D1 concerned to performing data write-in procedure as shown in drawing 5 on real time at AV monitor section 19 while transmitting image voice data D1A to the hard disk controller 9 in the ATA hard disk drive section 5 at the time of data writing.

[0051] That is, CPU2 is the alternate status / device control register R6 among the control block registers RB in the hard disk controller 9 first. The hard disk corresponding to the device select code concerned is chosen by setting up a device select code from the hard disk drives which have a two or more kinds device select-code setting up function, such as a device 0, a device 1, etc. which are contained by the mechanical section 12 in (step SP1) and the ATA hard disk drive section 5.

[0052] then, the hard disk controller 9 -- the status / command SUREJISUTA R5 CPU2 after setting both the inner values of BSY (busy bit) and DRQ (data request bit) as "0" -- receiving -- condition signal DIORDY which can be outputted and inputted It sends out (step SP 2). Incidentally it means that setting processing of a status code ended BSY at the time of a value "0", and DRQ is the status / command SUREJISUTA R5 at the time of a value "0". It means that receive and it is not [correspondence] ready for the data transfer demand of the host CPU. Moreover, condition signal DIORDY which can be outputted and inputted Throughout [nascent state / of a data readout signal (IOR-) and a data write-in signal (IOW-)] needs to be active, and it is used for data transfer generating an access weight signal logically to inactive and the intermediary host CPU at the time of ***** inside a disk drive.

[0053] CPU2 is the status / command register R5 in the hard disk controller 9. Or repeat the alternate status register R6 with the same contents by loop-formation processing, and read-out processing is performed. After checking the written-in status code, BSY=0, and DRQ=0 (step SP 3), It is the sector count register R3 about all the numbers of sector counters of a transfer schedule. While setting up (step SP 4), a logic block address is specified one by one in the sector unit concerned, and it is the logic block-address register R4. It sets up (step SP 5). Thereby, the command block register RA and the control block register RB are set as write-in operating state.

[0054] Then, CPU2 is the status / command register R5. From writing in write-in command code, after setting up the value of each register of the command block register RA and the control block register RB (step SP 6), predetermined time (for example, ATA standard 400 [ns]) progress is carried out, and the value of each register concerned is stabilized (step SP 7). The hard disk controller 9 is the status / command register R5 in this. From detecting the written-in write-in command code, the memory address generating section 13 is set as the condition which can be operated.

[0055] then, CPU2 after both the hard disk controllers 9 set the value of "0" and DRQ as "1" for the value of BSY in the status / command register R5 -- receiving -- condition signal DIORDY which can be outputted and inputted It sends out (step SP 9). CPU2 is the status / command register R5 in the hard disk controller 9. Or the alternate status register R6 with the same contents is repeated by loop-formation processing, read-out processing is performed, and the status code written in the register is repeatedly read until it is set to BSY=0 and DRQ=1 (step SP 10).

[0056] After this, CPU2 starts a data transfer to the hard disk controller 9, and transmits the image voice data D1 to the hard disk controller 9 per 1 sector first (step SP 11). The hard disk controller 9 is the sector KANUTO register R3. The sector number of counts, and the status/command register R5 Based on command code, (step SP12) and the image voice output data division 6 start the writing of the image voice data D1 supplied from CPU2 based on the memory address data DMA by generating the memory address data DMA of 1 sector (step SP 13).

[0057] the image voice data D1 for 1 sector supplies the hard disk controller 9 from CPU2 -- having -- ***** -- if things are checked -- interrupt-processing demand signal DINTRQ It generates and sends out to CPU2 (step SP 14).

[0058] CPU2 is the interrupt-processing demand signal DINTRQ. It is based and they are the status / command register R5 in the hard disk controller 9. The status code corresponding to the written-in following sector is read (step SP 15). It responds to this and the hard disk controller 9 is the interrupt-processing demand signal DINTRQ. A check of having cleared performs the same data write-in processing as steps SP11-SP13 (step SP 14). Thus, while CPU2 performs data transfer for every sector one by one, the hard disk controller 9 continues sending out the memory address data DMA to the image voice output data division 6 per sector.

[0059] The hard disk controller 9 is the sector count register R3. When it judges that it was based and all the sector numbers of counts were completed, they are the status / command register R5. Both the inner values of BSY and DRQ are set as "0" (step SP 30). Thereby, the hard disk controller 9 suspends generating of the memory address data DMA, and the image voice output data division 6 end the writing of the image voice data D1 (step SP 31). The hard disk controller 9 is the interrupt-processing demand signal DINTRQ in this. It generates (step SP 31) and this is sent out to CPU2 (step SP 32).

[0060] CPU2 is the interrupt-processing demand signal DINTRQ. When popularity is won, they are the status / command register R5 in the hard disk controller 9 in order to check all data transfer termination. The written-in status code is read (step SP 33). The hard disk controller 9 is the interrupt-processing demand signal DINTRQ in this. The data write-in procedure concerned is ended by clearing.

[0061] (3) In actuation of the gestalt of this operation, and the configuration beyond effectiveness, with this hard disk drive unit 1, CPU2 writes in the image voice data D1 supplied from the image voice data generation section 3 corresponding to the specified address concerned while specifying the address according to address data DAD to each register in the hard disk controller 9 in the ATA hard disk drive section 5.

[0062] At this time, if the hard disk controller 9 supplies the address data DAD according to each registers RA and RB to the memory address generating section 13 by the word unit, the memory address generating section 13 will carry out sequential generation of the memory address data DMA according to the 1st and 2nd bank memory 16 and 17 by the word unit based on the address data DAD concerned.

[0063] Thus, changing the address data DAD according to each registers RA and RB into the memory address data DMA according to the 1st and 2nd bank memory 16 and 17 To each registers RA and RB in the hard disk controller 9 As opposed to repeating the image voice data D1 to the same address position per sector, and writing it in it to the 1st bank memory 16 or 2nd bank memory 17 in the image voice data output section 6 It is because the image voice data D1 is written in the address position which accumulation was carried out one by one and increased by the word unit.

[0064] The memory address generating section 13 sends out the memory address data DMA of a word unit by turns to the 1st bank memory 16 or 2nd bank memory 17 in the image voice data output section 6. Thereby, while the address [bank memory / 1st / bank memory 16 or 2nd bank memory 17] according to the memory address data DMA by turns is specified, the image voice data D1 is written in per frame.

[0065] Thereby, in case CPU carries out data transfer of the image voice data D1 to the hard disk controller 9, synchronizing with the timing of the data transfer concerned, data transfer of it can be carried out to the 1st bank memory 16 or 2nd bank memory 17 of the image voice output data division 6.

[0066] While writing data in one memory per frame among the 1st bank memory 16 or the 2nd bank memory 17 furthermore, by having made it repeat by turns the actuation which reads data from the memory of another side in a frame unit, and is sent out to AV monitor section 19, the monitor display of the image voice data can be carried out on the write-in processing and real time over a disk drive.

[0067] According to the above configuration, in this hard disk drive unit 1 After CPU2 specifies the address according to address data DAD to each registers RA and RB in the hard disk controller 9, Based on the address concerned, generate the address corresponding to the 1st bank memory 16 and 2nd bank memory 17 in the image voice data output section 6, and the generated address concerned is specified by turns. While writing the image voice data D1 in one side per frame among the 1st bank memory 16 or the 2nd bank memory 17 By reading the image voice data D1 from another side per frame, and having

been made to carry out a screen display to AV monitor section 19 It synchronizes with the timing which writes the image voice data D1 in the hard disk in the mechanical section 12. The written-in image voice data D1 concerned can be expressed in AV monitor section 19 as real time, and the hard disk drive unit 1 which may improve a transfer rate markedly in this way can be realized.

[0068] (4) it is the gestalt of other operations -- the gestalt of above-mentioned operation -- setting -- the 1st and 2nd bank memory 16 and 17 in the image voice data output section 6 as 2nd storage control means -- receiving -- Although the case where it addressed to every 128[kbyte] and data transfer was made to be carried out was described Not only this but the 1st and 2nd bank memory 16 and 17 is divided into the partition of a predetermined number, respectively, and you may make it this invention specify and write a memory address in each partition concerned repeatedly one by one.

[0069] For example, as shown in drawing 6 (A), when addressing and carrying out data transfer to every 16[kbyte], 1 image block can be formed by dividing and transmitting the image voice data D1 of every [which is read from the 1st or 2nd bank memory 16 and 17] 16[kbyte] to a predetermined number (drawing 6 (B)). Moreover, the address number of bits needed for the memory address data DMA outputted from the memory address generating section 13 in this case can be reduced to 14 bits (the gestalt of incidentally operation 19 bits).

[0070] Moreover, in the gestalt of above-mentioned operation, although the case where a screen display was outputted and carried out to AV monitor section 19 as a display means was described while writing the image voice data D1 in the hard disk drive unit 1 therefore at the hard disk, this invention is applicable also about the case where this invention reads not only this but the image voice data D1 from a hard disk.

[0071] in this case, the step SP 7 mentioned above in the data readout procedure shown in drawing 7 which gave the same sign to the corresponding point with drawing 5 -- then, a hard disk controller -- the status / command register R5 CPU2 after setting both the values of "0" and DRQ as "1" for the value of inner BSY (step SP 9) -- receiving -- interrupt-processing demand signal DINTRQ It generates (step SP 40). CPU2 is the interrupt-processing demand signal DINTRQ. When popularity is won, they are the status / command register R5 in the hard disk controller 9. The written-in status code is read (step SP 41).

[0072] The hard disk controller 9 is the interrupt-processing demand signal DINTRQ after this. If it checks having cleared (step SP 40), CPU2 will start a data transfer to the hard disk controller 9, and will transmit the image voice data D1 to the hard disk controller 9 per 1 sector (step SP 42). The hard disk controller 9 is the sector KANUTO register R3. The sector number of counts, and the status/command register R5 Based on command code, (step SP43) and the image voice output data division 6 start the writing of the image voice data D1 supplied from CPU2 based on the memory address data DMA by generating the memory address data DMA of 1 sector (step SP 44).

[0073] the image voice data D1 for 1 sector supplies the hard disk controller 9 from CPU2 -- having -- ***** -- if things are checked -- interrupt-processing demand signal DINTRQ It generates and sends out to CPU2 (step SP 45). CPU2 is the interrupt-processing demand signal DINTRQ. It is based and they are the status / command register R5 in the hard disk controller 9. The status code corresponding to the written-in following sector is read (step SP 46). It responds to this and the hard disk controller 9 is the interrupt-processing demand signal DINTRQ. A check of having cleared performs the same data write-in processing as steps SP42-SP44 (step SP 45). Thus, while CPU2 performs data transfer for every sector one by one, the hard disk controller 9 continues sending out the memory address data DMA to the image voice output data division 6 per sector.

[0074] The hard disk controller 9 is the sector count register R3. When it judges that it was based and all the sector numbers of counts were completed, they are the status / command register R5. Both the inner values of BSY and DRQ are set as "0" (step SP 60), and it is judged that all data transfer completion was similarly carried out. CPU2 reads the status / command register R5 (step SP 61). With this, the hard disk controller 9 suspends generating of memory address data, and while the image voice output data division 6 end the writing of the image voice data D1 (step SP 62), the hard disk controller 9 ends the data readout procedure concerned.

[0075] Thus, while reading the image voice data D1 from a hard disk to a hard disk drive unit 1 therefore by performing data readout procedure, a screen display can be outputted and carried out to AV monitor section 19.

[0076] Furthermore, it sets in the gestalt of above-mentioned operation, and is the interrupt-processing demand signal DINTRQ for every sector transfer. Although the PIO (Programmed I/O) transfer to generate was described, this invention is a DMA transfer given not only in it being able to come but a standard [for ATA/ATAPI] one, and Ultra. It is applicable also to a DMA transfer and the future-extension method which is an ATA/ATAPI standard method further.

[0077] Although the case where the hard disk controller 9 as 1st storage control means and the memory address generating section 13 as an address-generation means were formed in another object was furthermore described in the gestalt of above-mentioned operation, you may make it this invention prepare not only this but the hard disk controller 9 and the memory address generating section 13 in one.

[0078] Although the case where a hard disk was applied as a record medium which writes in the image voice data D1 was furthermore described in the gestalt of above-mentioned operation, in addition to this, this invention is widely applicable not only to this but various devices, such as CD-ROM and a magnetic tape. That is, other equipments other than hard disk drive unit 1 can be applied as a data processor.

[0079]

[Effect of the Invention] The 1st step which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside according to this invention as mentioned above, The 2nd step which generates the 2nd address corresponding to the 2nd storage means based on the 1st address specified as the 1st storage means, The 3rd step which specifies the 2nd address as the 2nd storage means, and memorizes image data for every frame, By having prepared the 4th step which reads and carries out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium Synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame, and the data-processing approach which may improve a transfer rate markedly in this way can be realized.

[0080] Moreover, the 1st storage control means which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied from the outside for every frame in this invention, An address-generation means to generate the 2nd address corresponding to the 2nd storage means based on the 1st address therefore specified as the 1st storage control means, The 2nd storage control means which specifies the 2nd address therefore generated at the address-generation means as the 2nd storage means, and memorizes image data for every frame, The write-in means which reads image data from the 1st storage means for every frame, and is written in a record medium, By having established a display means by which a write-in means read and carried out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium Synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame, and the data processor which may improve a transfer rate markedly in this way can be realized.

[Translation done.]

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
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TECHNICAL FIELD

[Field of the Invention] This invention is applied to the hard disk drive unit which performs the writing and read-out of image voice data, concerning the data-processing approach and a data processor, and is suitable.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] the whole surface or the thing which boiled on the other hand, carries out the data compression of the image voice data by making it correspond if needed, respectively on both sides of each hard disk concerned, and was recorded of a hard disk is used, respectively in the magnetic head attached at the tip of two or more movable arms, carrying out high-speed rotation of two or more hard disks on a coaxial core as this kind of a hard disk drive unit conventionally.

[0005] A track is formed in both sides of each [these] hard disk concentric circular, respectively, and ** or an intermediary track number is assigned to the most inner circumference from the outermost periphery. Furthermore, each track is divided into the sector which makes a predetermined data length a unit, and the logic block address (LBA) as a sector number is assigned to each sector concerned.

[0006] In this hard disk drive unit, CPU sets the sector number of counts showing the count of a sector transfer of each sector concerned as a data register while specifying the data register prepared in the disk drive according to the logic block address assigned for every sector of a predetermined hard disk.

[0007] Then, CPU is made as [write / for every frame / image voice data], carrying out sequential addressing of a series of image voice data which consists of two or more sectors to the data register in a disk drive, after writing each data block in each buffer memory of a bank-switching method in order of FIFO (First In First Out) by turns one by one for every [for every 1 image voice data block] frame.

[0008] Then, CPU is made as [output / to the monitoring device by which read from the memory concerned and external connection was made if needed], after writing in for every frame, carrying out sequential addressing of the image voice data read from buffer memory to the memory in which it was built by the image voice output circuit.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] The 1st step which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside according to this invention as mentioned above, The 2nd step which generates the 2nd address corresponding to the 2nd storage means based on the 1st address specified as the 1st storage means, The 3rd step which specifies the 2nd address as the 2nd storage means, and memorizes image data for every frame, By having prepared the 4th step which reads and carries out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium Synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame, and the data-processing approach which may improve a transfer rate markedly in this way can be realized.

[0080] Moreover, the 1st storage control means which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied from the outside for every frame in this invention, An address-generation means to generate the 2nd address corresponding to the 2nd storage means based on the 1st address therefore specified as the 1st storage control means, The 2nd storage control means which specifies the 2nd address therefore generated at the address-generation means as the 2nd storage means, and memorizes image data for every frame, The write-in means which reads image data from the 1st storage means for every frame, and is written in a record medium; By having established a display means by which a write-in means read and carried out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium Synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame, and the data processor which may improve a transfer rate markedly in this way can be realized.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, CPU is **** in ****, if image voice data is not transmitted per frame, respectively, carrying out sequential assignment of the address which cannot specify [as opposed to / when carrying out data transfer of a series of image voice data stored in buffer memory to both a disk drive and an image voice output circuit at coincidence / the data register in a disk drive, and the memory in an image voice output circuit] the same address directly, but is mutually different.

[0010] Moreover, for CPU, the processing time when setting up various registers other than the data register in the disk drive concerned before starting data transfer to a disk drive, until the set point of the register concerned is decided is about 100-300 each time. It was once in every [ns]. Furthermore, when data interruption was processed two or more times after CPU ended data transfer to the disk drive, it required once the processing time before and behind about 5-10 [mus] for whenever [the].

[0011] For this reason, when data transfer of a series of image voice data was carried out continuously, in consideration of a register setup and interrupt processing which were mentioned above being performed, it was made as [make / the image voice data concerned / transmit for every frame unit within predetermined time amount (for example, 128 [kbyte] less than 33 [ms] and another example 512 [kbyte] less than 0.5 [ms])].

[0012] Therefore, when data transfer is made to once start to a disk drive, CPU is **** in ****, if image voice data must be transmitted to a data register for every frame unit and image voice data of each frame unit is not transmitted to memory to an image voice output circuit next, without stopping on the way. Consequently, the problem of taking the data transfer time to a disk drive and an image voice data output circuit for a long time, respectively is *****.

[0013] In case data transfer of the CPU is carried out to a disk drive, furthermore, within a disk drive Retry (rewrite) actuation, When transfer operation, such as a jump between tracks on a hard disk or a jump between sectors; etc. is performed, Condition signal DIORDY at the time of performing data transfer from a disk drive at the time of each actuation concerned which can be outputted and inputted Use and the signal is stopped temporarily, The waiting demand signal for access for keeping the access processing from CPU waiting temporarily indicated by the ATA standard method is emitted. These above results, CPU is **** in ****, if it carries out with a data transfer rate more nearly high-speed than the usual data transfer rate and data transfer which continued by another processing in another side and an image voice output circuit is not performed in a hard disk, in order to perform discontinuous data transfer in time to a disk drive and to perform a real-time operation for this reason.

[0014] For this, the problem of being hard to judge on real time whether data transfer [as opposed to / the data transfer to a disk drive will be processed not by real time but by another time amount, and / a disk drive in CPU] having been performed certainly is *****.

[0015] This invention was made in consideration of the above point, and tends to propose the data-processing approach and data processor which may improve a transfer rate markedly.

[Translation done.]

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MEANS

[Means for Solving the Problem] In order to solve this technical problem, it sets to this invention. The 1st step which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied for every frame from the outside, The 2nd step which generates the 2nd address corresponding to the 2nd storage means based on the 1st address specified as the 1st storage means, The 3rd step which specifies the 2nd address as the 2nd storage means, and memorizes image data for every frame, and the 4th step which reads and carries out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium were prepared. [0017] Consequently, synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame.

[0018] Moreover, the 1st storage control means which specifies the 1st address as the 1st storage means one by one, and memorizes the image data supplied from the outside for every frame in this invention, An address-generation means to generate the 2nd address corresponding to the 2nd storage means based on the 1st address therefore specified as the 1st storage control means, The 2nd storage control means which specifies the 2nd address therefore generated at the address-generation means as the 2nd storage means, and memorizes image data for every frame, The write-in means which reads image data from the 1st storage means for every frame, and is written in a record medium, and a display means by which a write-in means read and carried out a screen display of the image data for every frame from the 2nd storage means synchronizing with the timing written in a record medium were established.

[0019] Consequently, synchronizing with the timing which writes image data in a record medium for every frame, a screen display of the written-in image data concerned can be carried out on real time for every frame.

[0020]

[Embodiment of the Invention] About a drawing, the gestalt of 1 operation of this invention is explained in full detail below.

[0021] (1) In the whole hard disk drive unit block diagram 1, 1 shows the hard disk drive unit which consists of a standard ATA (AT attachment) method of an IDE (intelligent drive electronics) interface as a whole, and is made as [carry out /, respectively / through the host bus 4 / at the ATA hard disk drive section 5 and the image voice data output section 6 / to CPU2 / data transfer of the image voice data D1 by which sequential supply is therefore carried out from the image voice data generation section 3].

[0022] The ATA interface section 7 is formed between the host bus 4 and the ATA hard disk drive section 5, and it is made as [give / through the ATA drive interface section 8 in the ATA hard disk drive section 5 / the various data supplied from CPU2 and the image voice data generation section 3 / the hard disk controller 9].

[0023] Moreover, the controller interface section 10 is formed between the host bus 4 and the image voice data output section 6, and it is made as [give / the various data supplied from CPU2 and the image voice data generation section 3 / the register set section 11 in the image voice data output section 6].

[0024] This host bus 4 consists of address bus 4A, data bus 4B, and control bus 4C. Among these,

address bus 4A is a bus for giving the address data DAD for specifying the address of the various registers sent out from CPU2 to the ATA interface section 7 and the controller interface section 10.

[0025] Moreover, data bus 4B is a bus for giving the image voice data D1 supplied from the image voice data generation section 3 to the ATA interface section 7 and the controller interface section 10.

[0026] Furthermore, control bus 4C is CDC DCON for controlling the data transfer to each register in the ATA hard disk drive section 5 sent out from CPU2. While giving the ATA interface section 7, when the timing of the data transfer concerned becomes discontinuous, in order that the ATA hard disk drive section 5 may suspend data transfer temporarily, it is a bus for sending out the weight signal DWA to CPU2. In addition, this control bus 4C is the ATA hard disk drive section 5 concerned to the interrupt-processing demand signal DINTRQ, when the data transfer to each register in the ATA hard disk drive section 5 is completed. While sending out to CPU2, when it is in a condition accessible in the case of the data transfer concerned, it is the condition signal DIORDY which can be outputted and inputted from the ATA interface section 7 and the controller interface section 10. It is also a bus for sending out to CPU2.

[0027] The hard disk controller 9 in the ATA hard disk drive section 5 has the command block register RA and the control block register RB, and specifies them here according to the address assigned based on the address data DAD to which each registers RA and RB concerned were supplied from CPU2 for every sector of the predetermined hard disk in the mechanical section 12 (not shown).

[0028] At this time, the ATA interface section 7 is made as [specify / to the command block register RA and the control block register RB in the hard disk controller 9 / the address according to address data DAD] by performing predetermined address translation processing to the address data DAD supplied through address bus 4A from CPU2.

[0029] Specifically, address data DAD consist of two or more address A0 -A10 expressed with 32 bits of a hexadecimal notation, respectively, as shown in drawing 2 (A). Address A1 -A10 of these plurality are changed into the address corresponding to the command block register RA and the control block register RB through the ATA interface section 7.

[0030] The address after conversion is shown in drawing 2 (B), and, therefore, it is expressed 1-bit "CS0 -" and "CS1 -" to "DA (device address)" of a triplet, among these "CS0 -" and "CS1 -" are the addresses for choosing the register which both serves as a candidate for a setting out of two or more registers.

Address A1 -A8 among two or more address A1 -A10 actually based on address data DAD "CS0 -" is a value "0", and "CS1 -" expresses a value "1", and the command block register RA is chosen at this time. Moreover, address A9 And "CS0 -" is a value "1", and, as for A10, "CS1 -" expresses a value "0", and the control block register RB is chosen at this time.

[0031] Moreover, "DA" shows eight kinds of device addresses from "0h" to "7h" expressed with the triplet of a hexadecimal notation, and the class of each register which constitutes the command block register RA or the control block register RB corresponding to these device addresses is chosen.

[0032] In this command block register RA, they are a data register R1, the error / feature register R2, the sector count register R3, and the logic block-address register R4. And the status / command register R5 It is and they are the alternate status / device control register R6 in the control block register RB. And non-used register R7 It is. Data register R1 It is other register R2 -R7 to writing or read-out being possible at a word unit. Writing or read-out is possible per cutting tool register.

[0033] two or more address A0 -A10 based on address data DAD in this way constitute the command block register RA and the control block register RB -- each -- register R1 -R7 It is changed into the address to which it responded:

[0034] the magnetic head attached at the tip of two or more movable arms (not shown) while the mechanical section 12 (drawing 1) carried out high-speed rotation of the basis of control of the hard disk controller 9, and two or more hard disks (not shown) on the coaxial core -- respectively -- the whole surface of a hard disk -- or on the other hand, it be alike, and it be made to correspond and be made as [perform / , respectively / to both sides top of each hard disk concerned / the writing or read-out of the image voice data D1].

[0035] It is the sector count register [in / on drawing 3 and / in the hard disk controller 9 / the command

block register RA] R3. All the sector numbers of counts, and the status/command register R5 Command code is given to command code section 13A in the memory address generating section 13, data write-in counter 13B, and sector counter 13C.

[0036] Thereby, command code section 13A is the sector count register R3. The sector number of counts, and the status/command register R5 Write-in command code is judged, the writing of the command codes (for example, WRITE SECTORS (30h), WRITE DMA (CAh), etc.) which are write-in system commands is detected, and the memory address generating section 13 whole is set as the condition which can be operated.

[0037] Moreover, data write-in counter 13B is the sector count register R3. The sector number of counts, and the status/command register R5 Sequential generation of the address corresponding to the data in each logical sector according to each specified logic block address is carried out by the word unit. Sector counter 13C detects the count of carry actuation of the counter predicted in data write-in counter 13B, or is the sector count register R3. The count of subtraction count actuation is detected and sequential generation of the address which comes to add the count of actuation per sector (512 [byte] units) is carried out.

[0038] Memory address composition section 13D undergoes the output which it comes to count up in data write-in counter 13B and sector counter 13C, respectively, adds these addresses, and gives them to the image voice output controller 15 in the image voice data output section 6 through the memory address interface 14 as memory address data DMA.

[0039] In addition, after the memory address data DMA of the image voice data of the 1-block unit which continues from memory address composition section 13D are send out to the image voice output controller 15, the memory address generating section 13 detects the data write-in condition to a command register RA, clears data write-in counter 13B and sector counter 13C according to the detection result concerned, and performs an address count again.

[0040] Or in the image voice data based on MPEG 2 specification, I picture data and voice data are gathered to a part of several minutes of the beginning here. To write in and read ***** and a part of several minutes of the beginning for the remainder in the case of variable-length size data for disks rearranged in order of P picture data and B picture data By writing the partition of an eye in the memory address which carried out sequential assignment partly from the beginning, after dividing the 1st or 2nd bank memory 16 and 17 in the image voice data output section 6 into the partition of a predetermined number if needed The continuous image voice data D1 is written in the 1st or 2nd bank memory 16 and 17 within 1 image block unit.

[0041] At this time, after the synthetic result of the output obtained from data write-in counter 13B and sector counter 13C generates the address in the range which is partly equivalent only to the partition of an eye from the beginning among the partitions of a predetermined number, clear reset of the AV memory partition counter 13E is carried out, it stops the address generation concerned, and ends the data transfer of the hard disk controller 9. In addition, the hard disk controller 9 is the sector count register R3 in this case. When the sector number of counts of the count of predetermined carries out transfer termination, it may be made to carry out clear reset.

[0042] Thus, the memory address generating section 13 responds to the address based on the address data DAD sent out from CPU2, and is the predetermined register R3 in the hard disk controller 9. And R5 After generating the memory address data DMA mentioned above based on the specified each address concerned after carrying out sequential assignment by the word unit one by one, this is supplied to the image voice output controller 15.

[0043] Moreover, the register set section 11 in the image voice data output section 6 is the address data DAD and CDC DCON which are sent out through the host bus 4 and the controller interface section 10 one by one from CPU2. It is [whether it was based and was set to the condition in which data transfer is possible to the image voice output controller 15, and] the set condition data DSET. It sends out.

[0044] The image voice output controller 15 is the set condition data DSET. When it expresses that it is in the condition in which data transfer is possible, the memory address data DMA supplied by the word unit one by one are sent out to the 1st bank memory 16 or 2nd bank memory 17 by turns, and sequential

assignment of the 1st bank memory 16 or 2nd bank memory 17 is carried out according to the memory address based on the memory address data DMA, respectively.

[0045] The maximum number of transfer data which can be transmitted at 1 time of the memory address data DMA in the case of the gestalt of this operation as incidentally shown in drawing 4 (A) It is 128 [kbyte]. Namely, sector count register R3 Since it is 8-bit width of face, it is the sector count register R3 of 8-bit width of face. Setting maximum is 256. It becomes the set point of the count of a sector transfer of a time. Therefore, the data of 1 sector of the hard disk controller 9 are based on 256 WORD data transfer of 1 word = 2[byte]. Since it is 512 [byte], the memory address data DMA are max. It considers as 1 transfer block unit which can set up the data size of 128 [kbyte] (256 time x 512[byte]), and is transmitted to the 1st bank memory 16 or 2nd bank memory 17. In addition, as shown in drawing 4 (B), it is one frame (1 image block). When consisting of 512 [kbyte], it is repeatedly read from the 1st bank memory 16 or 2nd bank memory 17 by turns one by one. It is made as [form / the image voice data D1 of every 128[kbyte] is collected 4 times, and / 1 image block].

[0046] Thereby, the image voice data D1 supplied through the register set section 11 is written in the 1st bank memory 16 or 2nd bank memory 17 by turns per frame corresponding to the memory address by which sequential assignment was carried out. While writing the image voice data D1 for one frame in one memory among the 1st bank memory 16 or the 2nd bank memory 17 at this time, the image voice data D1 for one already written-in frame is read from the memory of another side, and it sends out to the decoder section 18.

[0047] After the decoder section 18 decodes the image voice data D1 given by turns for every frame from the 1st bank memory 16 or 1st bank memory 17, it is sent out to AV monitor section 19 for every frame by which the sequential input was carried out. the image and voice based on [in this way] the image voice data D1 at AV monitor section 19 -- a display -- and sound emission is carried out.

[0048] on the other hand, in not performing control which uses only the image voice data output section 6 independently, and writes image voice data in a hard disk 5 The image voice output controller 15 is the set condition data DSET given from the register set section 11. When it expresses that it is in the condition in which data transfer is impossible, CPU2, without supplying the image voice data D1 to the ATA hard disk drive section 5 CPU2 carries out sequential assignment of the memory address by turns by the word unit to the 1st bank memory 16 or 2nd bank memory 17 through the controller interface section 10 and the register set section 11 directly. It is made to correspond to the specified memory address concerned, and the image voice data D1 is written in by turns for every frame.

[0049] After the image voice data D1 supplied by turns for every frame is given to the decoder section 18 and decoded in the decoder section 18 concerned like the next above-mentioned case from the 1st bank memory 16 or 2nd bank memory 17, it is sent out to AV monitor section 19 for every frame by which the sequential input was carried out.

[0050] (2) Therefore, the data write-in procedure CPU 2 outputs the transmitted image voice data D1 concerned to performing data write-in procedure as shown in drawing 5 on real time at AV monitor section 19 while transmitting image voice data D1A to the hard disk controller 9 in the ATA hard disk drive section 5 at the time of data writing.

[0051] That is, CPU2 is the alternate status / device control register R6 among the control block registers RB in the hard disk controller 9 first. The hard disk corresponding to the device select code concerned is chosen by setting up a device select code from the hard disk drives which have a two or more kinds device select-code setting up function, such as a device 0, a device 1, etc. which are contained by the mechanical section 12 in (step SP1) and the ATA hard disk drive section 5.

[0052] then, the hard disk controller 9 -- the status / command SUREJISUTA R5 CPU2 after setting both the inner values of BSY (busy bit) and DRQ (data request bit) as "0" -- receiving -- condition signal DIORDY which can be outputted and inputted It sends out (step SP 2). Incidentally it means that setting processing of a status code ended BSY at the time of a value "0", and DRQ is the status / command SUREJISUTA R5 at the time of a value "0". It means that receive and it is not [correspondence] ready for the data transfer demand of the host CPU. Moreover, condition signal DIORDY which can be outputted and inputted Throughout [nascent state / of a data readout signal (IOR-) and a data write-in

signal (IOW-)] needs to be active, and it is used for data transfer generating an access weight signal logically to inactive and the intermediary host CPU at the time of ***** inside a disk drive.

[0053] CPU2 is the status / command register R5 in the hard disk controller 9. Or repeat the alternate status register R6 with the same contents by loop-formation processing, and read-out processing is performed. After checking the written-in status code, BSY=0, and DRQ=0 (step SP 3), It is the sector count register R3 about all the numbers of sector counters of a transfer schedule. While setting up (step SP 4), a logic block address is specified one by one in the sector unit concerned, and it is the logic block-address register R4. It sets up (step SP 5). Thereby, the command block register RA and the control block register RB are set as write-in operating state.

[0054] Then, CPU2 is the status / command register R5. From writing in write-in command code, after setting up the value of each register of the command block register RA and the control block register RB (step SP 6), predetermined time (for example, ATA standard 400 [ns]) progress is carried out, and the value of each register concerned is stabilized (step SP 7). The hard disk controller 9 is the status / command register R5 in this. From detecting the written-in write-in command code, the memory address generating section 13 is set as the condition which can be operated.

[0055] then, CPU2 after both the hard disk controllers 9 set the value of "0" and DRQ as "1" for the value of BSY in the status / command register R5 -- receiving -- condition signal DIORDY which can be outputted and inputted It sends out (step SP 9). CPU2 is the status / command register R5 in the hard disk controller 9. Or the alternate status register R6 with the same contents is repeated by loop-formation processing, read-out processing is performed, and the status code written in the register is repeatedly read until it is set to BSY=0 and DRQ=1 (step SP 10).

[0056] After this, CPU2 starts a data transfer to the hard disk controller 9, and transmits the image voice data D1 to the hard disk controller 9 per 1 sector first (step SP 11). The hard disk controller 9 is the sector KANUTO register R3. The sector number of counts, and the status/command register R5 Based on command code, (step SP12) and the image voice output data division 6 start the writing of the image voice data D1 supplied from CPU2 based on the memory address data DMA by generating the memory address data DMA of 1 sector (step SP 13).

[0057] the image voice data D1 for 1 sector supplies the hard disk controller 9 from CPU2 -- having -- ***** -- if things are checked -- interrupt-processing demand signal DINTRQ It generates and sends out to CPU2 (step SP 14).

[0058] CPU2 is the interrupt-processing demand signal DINTRQ. It is based and they are the status / command register R5 in the hard disk controller 9. The status code corresponding to the written-in following sector is read (step SP 15). It responds to this and the hard disk controller 9 is the interrupt-processing demand signal DINTRQ. A check of having cleared performs the same data write-in processing as steps SP11-SP13 (step SP 14). Thus, while CPU2 performs data transfer for every sector one by one, the hard disk controller 9 continues sending out the memory address data DMA to the image voice output data division 6 per sector.

[0059] The hard disk controller 9 is the sector count register R3. When it judges that it was based and all the sector numbers of counts were completed, they are the status / command register R5. Both the inner values of BSY and DRQ are set as "0" (step SP 30). Thereby, the hard disk controller 9 suspends generating of the memory address data DMA, and the image voice output data division 6 end the writing of the image voice data D1 (step SP 31). The hard disk controller 9 is the interrupt-processing demand signal DINTRQ in this. It generates (step SP 31) and this is sent out to CPU2 (step SP 32).

[0060] CPU2 is the interrupt-processing demand signal DINTRQ. When popularity is won, they are the status / command register R5 in the hard disk controller 9 in order to check all data transfer termination. The written-in status code is read (step SP 33). The hard disk controller 9 is the interrupt-processing demand signal DINTRQ in this. The data write-in procedure concerned is ended by clearing.

[0061] (3) In actuation of the gestalt of this operation, and the configuration beyond effectiveness, with this hard disk drive unit 1, CPU2 writes in the image voice data D1 supplied from the image voice data generation section 3 corresponding to the specified address concerned while specifying the address according to address data DAD to each register in the hard disk controller 9 in the ATA hard disk drive

section 5.

[0062] At this time, if the hard disk controller 9 supplies the address data DAD according to each registers RA and RB to the memory address generating section 13 by the word unit, the memory address generating section 13 will carry out sequential generation of the memory address data DMA according to the 1st and 2nd bank memory 16 and 17 by the word unit based on the address data DAD concerned.

[0063] Thus, changing the address data DAD according to each registers RA and RB into the memory address data DMA according to the 1st and 2nd bank memory 16 and 17 To each registers RA and RB in the hard disk controller 9 As opposed to repeating the image voice data D1 to the same address position per sector, and writing it in it to the 1st bank memory 16 or 2nd bank memory 17 in the image voice data output section 6 It is because the image voice data D1 is written in the address position which accumulation was carried out one by one and increased by the word unit.

[0064] The memory address generating section 13 sends out the memory address data DMA of a word unit by turns to the 1st bank memory 16 or 2nd bank memory 17 in the image voice data output section 6. Thereby, while the address [bank memory / 1st / bank memory 16 or 2nd bank memory 17] according to the memory address data DMA by turns is specified, the image voice data D1 is written in per frame.

[0065] Thereby, in case CPU carries out data transfer of the image voice data D1 to the hard disk controller 9, synchronizing with the timing of the data transfer concerned, data transfer of it can be carried out to the 1st bank memory 16 or 2nd bank memory 17 of the image voice output data division 6.

[0066] While writing data in one memory per frame among the 1st bank memory 16 or the 2nd bank memory 17 furthermore, by having made it repeat by turns the actuation which reads data from the memory of another side in a frame unit, and is sent out to AV monitor section 19, the monitor display of the image voice data can be carried out on the write-in processing and real time over a disk drive.

[0067] According to the above configuration, in this hard disk drive unit 1 After CPU2 specifies the address according to address data DAD to each registers RA and RB in the hard disk controller 9, Based on the address concerned, generate the address corresponding to the 1st bank memory 16 and 2nd bank memory 17 in the image voice data output section 6, and the generated address concerned is specified by turns. While writing the image voice data D1 in one side per frame among the 1st bank memory 16 or the 2nd bank memory 17 By reading the image voice data D1 from another side per frame, and having been made to carry out a screen display to AV monitor section 19 It synchronizes with the timing which writes the image voice data D1 in the hard disk in the mechanical section 12. The written-in image voice data D1 concerned can be expressed in AV monitor section 19 as real time; and the hard disk drive unit 1 which may improve a transfer rate markedly in this way can be realized.

[0068] (4) it is the gestalt of other operations -- the gestalt of above-mentioned operation -- setting -- the 1st and 2nd bank memory 16 and 17 in the image voice data output section 6 as 2nd storage control means -- receiving -- Although the case where it addressed to every 128[kbyte] and data transfer was made to be carried out was described Not only this but the 1st and 2nd bank memory 16 and 17 is divided into the partition of a predetermined number, respectively, and you may make it this invention specify and write a memory address in each partition concerned repeatedly one by one.

[0069] For example, as shown in drawing 6 (A), when addressing and carrying out data transfer to every 16[kbyte], 1 image block can be formed by dividing and transmitting the image voice data D1 of every [which is read from the 1st or 2nd bank memory 16 and 17] 16[kbyte] to a predetermined number (drawing 6 (B)). Moreover, the address number of bits needed for the memory address data DMA outputted from the memory address generating section 13 in this case can be reduced to 14 bits (the gestalt of incidentally operation 19 bits).

[0070] Moreover, in the gestalt of above-mentioned operation, although the case where a screen display was outputted and carried out to AV monitor section 19 as a display means was described while writing the image voice data D1 in the hard disk drive unit 1 therefore at the hard disk, this invention is applicable also about the case where this invention reads not only this but the image voice data D1 from a hard disk.

[0071] in this case, the step SP 7 mentioned above in the data readout procedure shown in drawing 7 which gave the same sign to the corresponding point with drawing 5 -- then, a hard disk controller -- the status / command register R5 CPU2 after setting both the values of "0" and DRQ as "1" for the value of inner BSY (step SP 9) -- receiving -- interrupt-processing demand signal DINTRQ It generates (step SP 40). CPU2 is the interrupt-processing demand signal DINTRQ. When popularity is won, they are the status / command register R5 in the hard disk controller 9. The written-in status code is read (step SP 41).

[0072] The hard disk controller 9 is the interrupt-processing demand signal DINTRQ after this. If it checks having cleared (step SP 40), CPU2 will start a data transfer to the hard disk controller 9, and will transmit the image voice data D1 to the hard disk controller 9 per 1 sector (step SP 42). The hard disk controller 9 is the sector KANUTO register R3. The sector number of counts, and the status/command register R5 Based on command code, (step SP43) and the image voice output data division 6 start the writing of the image voice data D1 supplied from CPU2 based on the memory address data DMA by generating the memory address data DMA of 1 sector (step SP 44).

[0073] the image voice data D1 for 1 sector supplies the hard disk controller 9 from CPU2 -- having --
***** -- if things are checked -- interrupt-processing demand signal DINTRQ It generates and sends out to CPU2 (step SP 45). CPU2 is the interrupt-processing demand signal DINTRQ. It is based and they are the status / command register R5 in the hard disk controller 9. The status code corresponding to the written-in following sector is read (step SP 46). It responds to this and the hard disk controller 9 is the interrupt-processing demand signal DINTRQ. A check of having cleared performs the same data write-in processing as steps SP42-SP44 (step SP 45). Thus, while CPU2 performs data transfer for every sector one by one, the hard disk controller 9 continues sending out the memory address data DMA to the image voice output data division 6 per sector.

[0074] The hard disk controller 9 is the sector count register R3. When it judges that it was based and all the sector numbers of counts were completed, they are the status / command register R5. Both the inner values of BSY and DRQ are set as "0" (step SP 60), and it is judged that all data transfer completion was similarly carried out. CPU2 reads the status / command register R5 (step SP 61). With this, the hard disk controller 9 suspends generating of memory address data, and while the image voice output data division 6 end the writing of the image voice data D1 (step SP 62), the hard disk controller 9 ends the data readout procedure concerned.

[0075] Thus, while reading the image voice data D1 from a hard disk to a hard disk drive unit 1 therefore by performing data readout procedure, a screen display can be outputted and carried out to AV monitor section 19.

[0076] Furthermore, it sets in the gestalt of above-mentioned operation, and is the interrupt-processing demand signal DINTRQ for every sector transfer. Although the PIO (Programmed I/O) transfer to generate was described, this invention is a DMA transfer given not only in it being able to come but a standard [for ATA/ATAPI] one, and Ultra. It is applicable also to a DMA transfer and the future-extension method which is an ATA/ATAPI standard method further.

[0077] Although the case where the hard disk controller 9 as 1st storage control means and the memory address generating section 13 as an address-generation means were formed in another object was furthermore described in the gestalt of above-mentioned operation, you may make it this invention prepare not only this but the hard disk controller 9 and the memory address generating section 13 in one.

[0078] Although the case where a hard disk was applied as a record medium which writes in the image voice data D1 was furthermore described in the gestalt of above-mentioned operation, in addition to this, this invention is widely applicable not only to this but various devices, such as CD-ROM and a magnetic tape. That is, other equipments other than hard disk drive unit 1 can be applied as a data processor.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the gestalt of 1 implementation of the configuration of the hard disk drive unit by this invention.

[Drawing 2] It is the graph with which explanation of the address translation processing by the ATA interface section by this invention is presented.

[Drawing 3] It is the block diagram showing the internal configuration of the hard disk controller by this invention, and the memory address generating section.

[Drawing 4] It is the approximate line Fig. showing the write-in condition to each bank memory by the gestalt of this operation.

[Drawing 5] It is the timing chart which shows the data write-in procedure by the gestalt of this operation.

[Drawing 6] It is the approximate line Fig. showing the write-in condition to each bank memory by the gestalt of other operations.

[Drawing 7] It is the timing chart which shows the data readout procedure by the gestalt of other operations.

[Description of Notations]

1 A hard disk drive unit, 2 .. CPU, 3 .. Image voice data generation section, 4A An address bus, 4B .. A data bus, 4C .. Control bus, 5 The ATA hard disk drive section, 6 .. Image voice data output section, 7 The ATA interface section, 9 .. Hard disk controller, 10 The controller interface section, 11 .. Register set section, 12 The mechanical section, 13 .. The memory address generating section, 15 .. Image voice output controller, 16 The 1st bank memory, 17 .. The 2nd bank memory, 18 .. Decoder section, 19 [.. Image voice data, DAD / .. Address data, DMA / .. Memory address data] AV monitor section, RA .. A command block register, RB .. A control block register, D1

[Translation done.]

* NOTICES *

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

[Drawing 2]

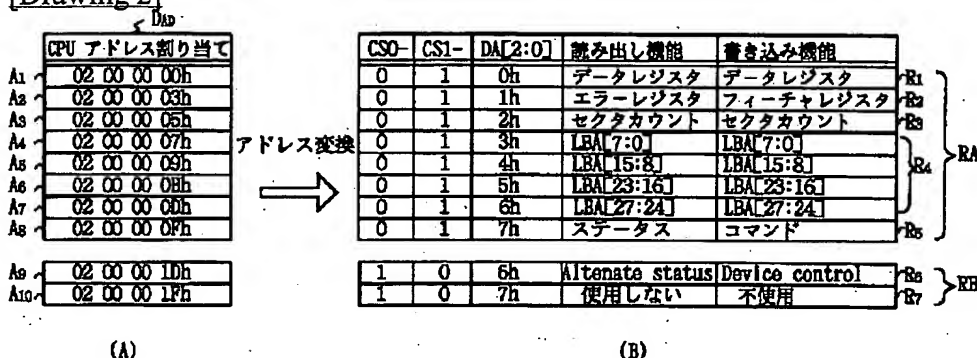


図2 ATAインタフェース部によるアドレス変換処理

[Drawing 1]

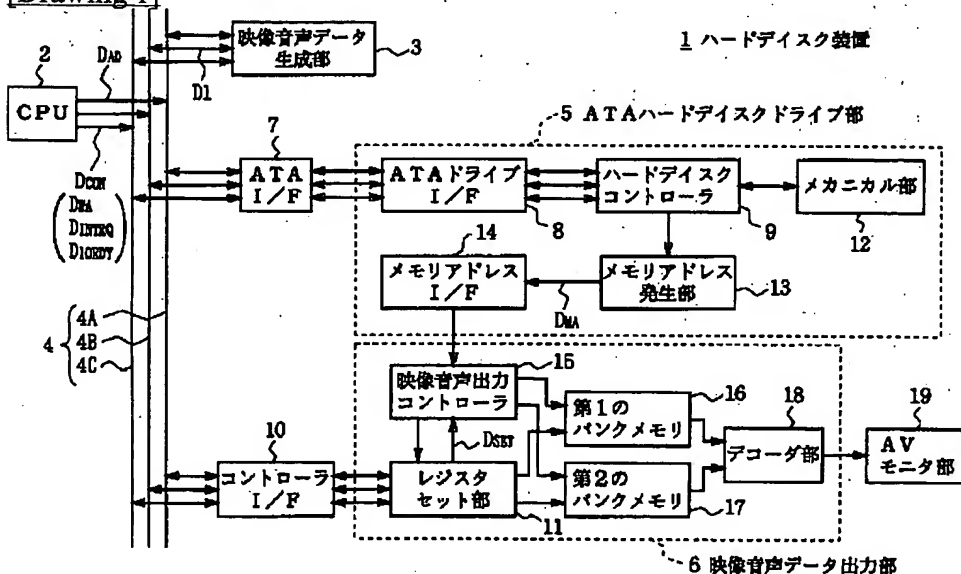


図1 本実施の形態によるハードディスク装置の構成

[Drawing 3]

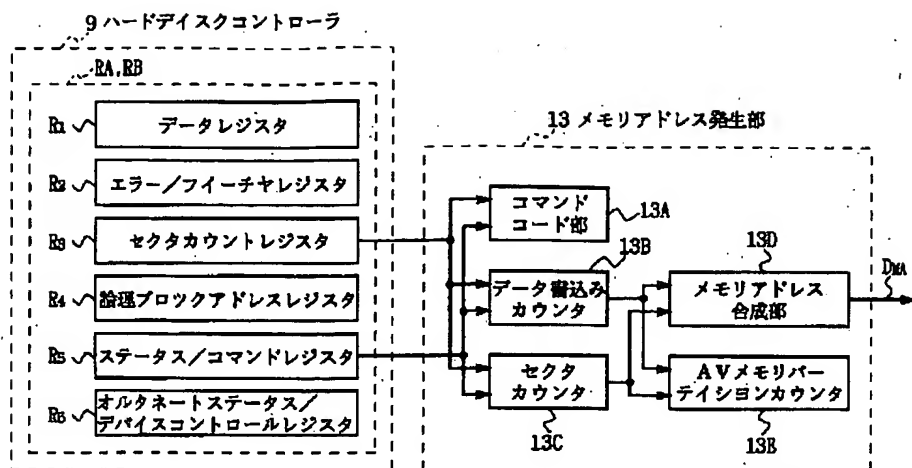


図3 ハードディスクコントローラ及びメモリアドレス発生部の内部構成

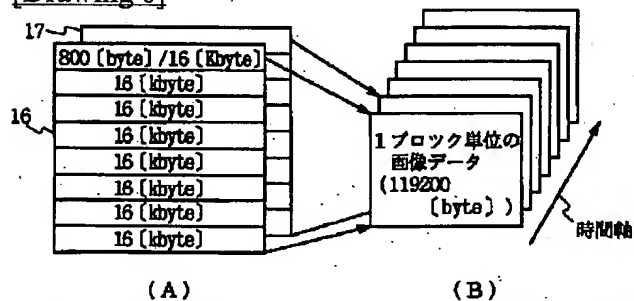
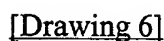


図6 他の実施の形態による各バンクメモリへの書き込み状態

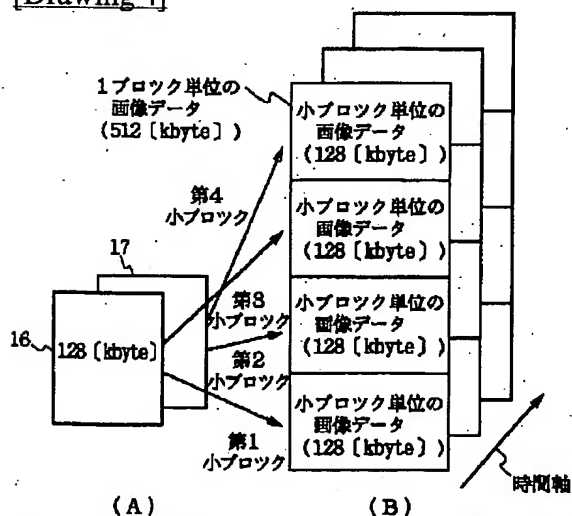
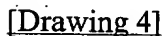
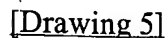


図4 本実施の形態による各バンクメモリへの書き込み状態



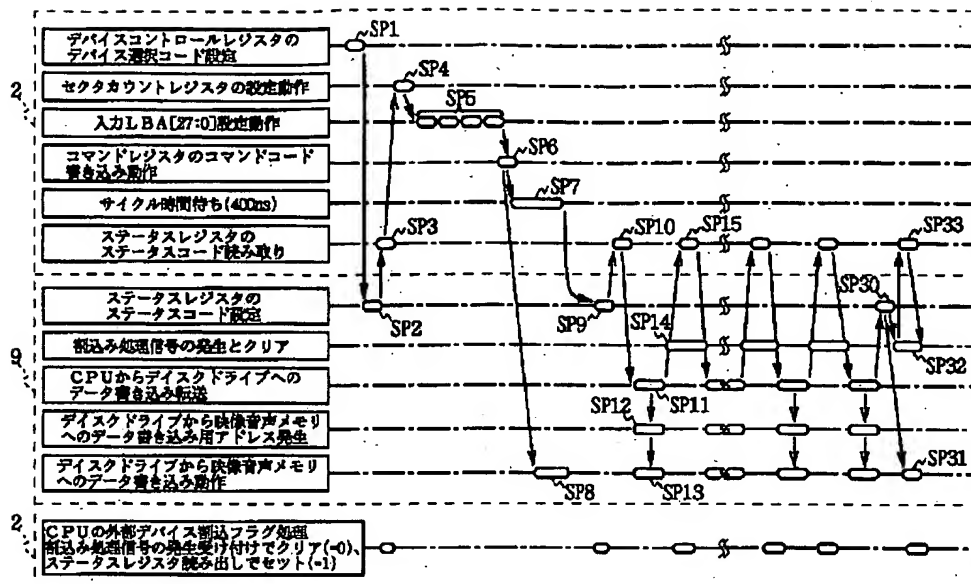


図5 本実施の形態によるデータ書き込み処理手順

[Drawing 7]

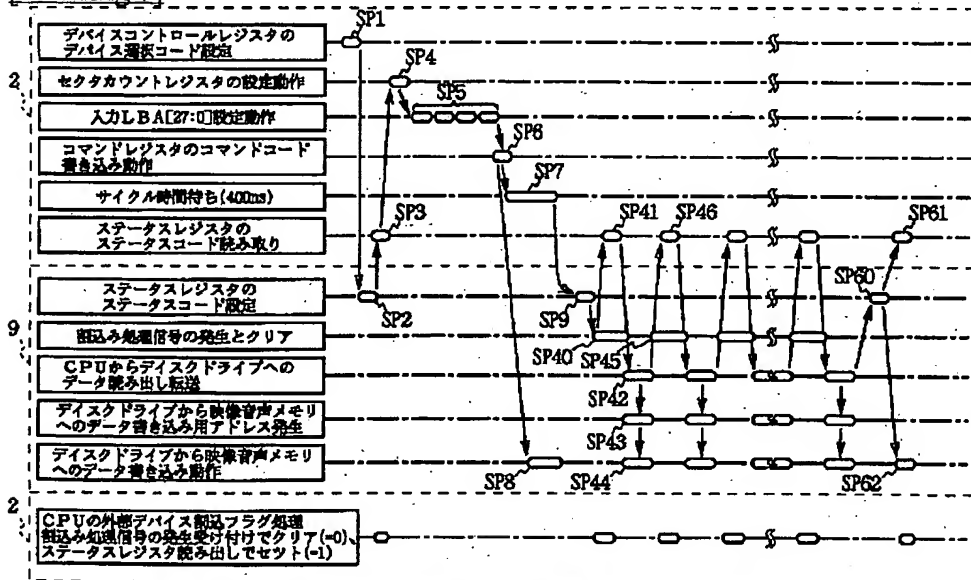


図7 他の実施の形態によるデータ読み出し処理手順

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